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Assessment of Cost Factors Impacting Planar Magnetic Windings

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***Abstract*—Planar magnetics are being actively explored in a wide range of power electronics applications, with argumentation of their low cost being a key aspect of their popularity. However, unlike conventional wire wound magnetic components, their costs do not scale convincingly with volume owing to a strong dependence on manufacturing complexity. This paper assesses the cost factors impacting the design of planar magnetic windings. This is done qualitatively, through direct manufacturer survey, and quantitatively by presenting a cost modelling approach derived from cost quotations of exemplar planar transformers. The developed model fits excellently to the data it was trained on (6.5% error). It is shown to have good predictive power on designs that are well-represented by the training data (though not in the training set, 13% error), and reasonable performance (20-58% error) on designs which have limited representation in the training data.**

***Index Terms*—Planar magnetics, cost model, PCB, optimization, manufacturing costs**

I. INTRODUCTION

Planar magnetics are inductors and transformers with windings that are implemented directly on printed circuit boards (PCBs). They represent an active area of research in high performance and miniaturized power conversion, owing to numerous advantages such as high repeatability, simplicity for manufacture, and improved thermals [1]. Another widely-touted feature of planar magnetics is their cost savings compared to wire-wound alternatives. This benefit is typically assessed qualitatively, for example, by noting the simpler manufacturing of printing the windings and slotting in a planar core compared to using a coil former to wind turns on a bobbin, mounting that bobbin on a core, and then installing the magnetic unit onto a PCB. Similarly, the cost impact of certain planar design choices, such as the number of layers, is also typically assessed qualitatively (e.g., by the reasonable assumption that a board with fewer layers will be less costly [2]–[4] or that some designs are complex to fabricate than others [5]).

Cost is an important metric in the trade-offs of considering a planar magnetic design. While the quotation from PCB manufacturers determines specific final costs, the ability to understand cost trends and estimate cost impacts in a planar magnetic design is of high utility.

For example, recent investigations have considered the use of planar magnetics in modular, grid-connected, solar photovoltaic (PV) conversion systems [6]. In these systems, an estimate of the levelized cost of electricity (LCOE) is fundamental to assessing the benefit of a new approach. However, because the literature does not contain a clear assessment of planar magnetic costs, existing LCOE optimizations have relied on conventional volume-scaled cost models which are poorly suited for planar magnetic windings [7]. Furthermore, the work in [7] has identified the transformer cost as critically impacting LCOE, emphasizing the importance of being able to identify it accurately.

Typical wire-wound magnetic components have costs that scale reasonably with volume since the primary materials that comprise the component, such as silicon steel and copper in a power transformer, are priced by weight (and by proxy, volume)[1]. In contrast, two planar magnetic components having similar volumes may have dramatically different costs, depending on the details and complexity of their manufacturing requirements.

Considerable works in power electronics include or discuss efficiency and power density as metrics of comparison between different typologies or designs [4], [8]–[11]. If passive component cost is modeled as proportional to volume, then the power density metric may also appear as a proxy for the cost of the passives in the design. It is noted that power density improvements in many applications are obtained by leveraging planar magnetics, which do not feature volume-scaled costs.

In volume-constrained applications such as electric vehicles [8], power density may also be argued to have an indirect cost benefit by the increased volume allocation which can be given to other elements of the system design. Similarly, smaller designs may enable lower system operating costs if the volume is taken as a proxy for weight. In applications not inherently volume-constrained, such as in the solar and grid sectors, volume reductions are typically pursued directly for their expected reductions on passive component costs [7]. In both cases, an improved assessment of planar magnetic costs is useful to enable better system-level design trade-offs.

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[1] Modifications to cost owing to specialized windings (e.g., Litz wire) or insulation materials, can also be readily estimated from manufacturer catalogues.

The literature on cost considerations in planar magnetics is sparse. The most relevant study is in [12] which formulates a cost-benefit analysis comparison between a planar and conventional transformer for a specific 100kHz power supply. However, this study does not provide a basis to compare two different planar magnetic components, and it does not consider constructions wound directly on a PCB (instead, it considers the historically more common implementation of planar magnetics in which the windings are implemented by multiple separate PCBs [13])[2]. Similarly, [14] offers a clear description of the process by which a manufacturer develops a PCB cost quote but does not offer quantitative insight into modern cost trends for planar magnetic windings.

In this paper, we clarify and quantify the key factors affecting the cost of planar magnetic windings in order to enable their cost-informed design. In doing so, we acknowledge that assessments of cost can be tenuous, as it is inherently affected by a multitude of economic factors which are difficult to control, including the local cost of labor, the impact of economies of scale, purchasing power of an entity (e.g., of an academic laboratory versus a multinational corporation), and the current state of the relevant supply chains. However, a clear, well-justified assessment of the relative cost impacts is a useful tool for researchers and designers who are exploring new planar magnetic architectures and configurations or who wish to leverage these components in cost-constrained systems. Our intent is not to provide exact price models for planar magnetics but to create a model allowing cost to *inform* their design and improve design comparison in literature studies where loss impact is widely used, but cost impact is lacking and volume reporting is not sufficient.

We identify eight key PCB design elements (illustrated in Fig. 1) that define a planar magnetic PCB winding. These variables are typically selected to minimize loss and/or volume of the component, and the goal of this work is to enable a designer to include the relative cost in this assessment if that is important to their design. This effort is motivated in part by the utility in connecting Litz wire cost to component performance described in [15]. To assess how these planar winding design elements impact cost, we first develop a qualitative summary by surveying PCB manufacturers based in the United States. Then, we develop a quantitative cost model by combining this information with a direct quotation of exemplar planar magnetics.

In Section II we discuss qualitative survey results for each PCB design element and describe a cost model which can be built from these responses. In Section III, we describe the cost data we obtained for this study then, in Section IV, we present our proposed cost model structure. The paper is concluded in Section V.

II. QUALITATIVE ASSESSMENT OF KEY COST FACTORS

The cost of manufacturing a PCB can be broadly partitioned into four categories: *labor* (payments to those responsible for manufacturing the PCB), *overhead* (auxiliary costs which keep the manufacturer and manufacturing facility operating), *materials* (costs of the raw materials comprising the PCB and the process materials used to manufacture it), and *scrap* (additional manufacturing costs owing to imperfect yield) [14]. These costs cannot be parsed directly from the weight or volume of a PCB. For example, a complicated PCB may use a similar amount of raw and process materials as a simpler one, but may involve higher labor and scrap costs. Furthermore, the specifics of these costs depend on the multitude of economic factors highlighted at the end of the introduction. In an effort to normalize the cost impacts of labor and overhead, we elected to survey manufacturers in a single geographic region (the U.S.). To normalize the effect of supply chains on material costs, the surveys were conducted within a three-week span. Detailed responses to our survey were received from five US-based PCB manufacturing houses. We also received more general feedback from three manufacturing houses, pointing to their own literature on cost factors or online calculators. The information obtained from this qualitative survey relates to the planar winding features illustrated in Fig. 1 and is summarized in Table I. The sections below provide additional details.

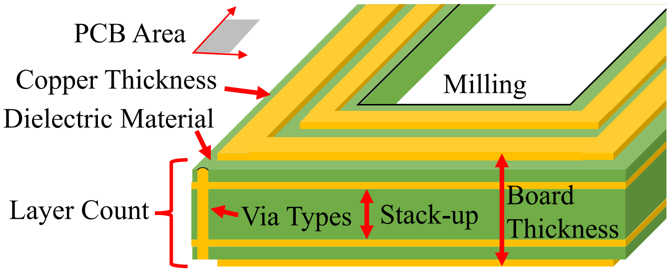

Fig. 1: Key planar magnetic winding features considered in the cost assessment.

TABLE I: Summary of PCB cost survey responses.

Feature	% increase in cost	Connection to planar winding design
Layer Count	35-40% for every additional layer pair (e.g., 4 to 6 layers)	Key driver of copper loss – affects the number of turns per layer, ability to interleave
Via Config.	20-30% increase for every additional via set	Strongly related to layer count and interleaving structure.
PCB Area	Scales with number of panels used (100% cost increase)	Board area is defined by the planar magnetic footprint.
Copper Thickness	10-20% for increasing from 1oz to 2oz	Related to winding loss.
Board thickness and Stack-up	Non-standard stack-ups cost more, too variable to generalize.	Typically specified to achieve a certain isolation requirement or to control interwinding capacitances.
Dielectric Material	10-60% depending on the material	Related to isolation requirements, loss, and board thickness.
Board Milling	0%	Related to core shape and isolation requirements. Stated to weakly affect cost.

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[2] Importantly, this study also indicates that the planar magnetic winding cost can be dominant, further emphasizing the importance of modeling it well.

A. Number of Layers

Question: We are interested in builds of 4, 6, 8, 10, and 12 layers. For all other aspects of the board held constant, is there a cost trend with varying the number of layers?

Summary of responses: For all other aspects of the board held constant, an increase of approximately 35-40% in price occurs for every two layers added to a four-layer board. This assessment was consistent across the manufacturer responses.

B. Via Types

Question: Can you comment on an approximate or quantitative cost trend for these different configurations? (1) Only through hole vias. (2) Through hole vias + blind vias only on the outer layers (e.g., from L1-L2 and L5-L6 in a 6 layer board)[3]*. (3) Through hole vias + blind vias + buried via connections so that every layer of the board has a path to every other layer.*

Summary of responses: The manufacturers generally assessed that an overall increase in cost of 20-30% would result for every additional set of vias beyond conventional through hole vias. One manufacturer directly commented that the base panel cost would double for every increase in via sets, but the net result on quoted price may still be in the stated range. Furthermore, it was assessed that exceeding three total drill layers was a critical point that would likely dramatically increase cost.

C. PCB Area

Question: How is cost affected by the area of the PCB design?

Summary of responses: The number of panels that are needed to complete an order is what dictates cost. Standard panel sizes are 12”x18” and 18”x24”, with corresponding image areas of 10”x16” and 22”x16”. The number of panels that are required depends on the area of the PCB design, the number of PCBs required, and the minimum spacing required between adjacent placements of the design on a panel (e.g., 0.25”). Tied to this is the complexity of a design (i.e., a high layer count, minimum trace width/spacing, and high trace count design would be more complex) – the more complicated a design is, the more panels must be processed to achieve the requisite yield.

D. Copper Thickness

Question: How does cost change if 1oz is used on all layers versus 2oz on all layers? If 3oz copper is used on outer layers with 2oz on inner layers?[4]

Summary of responses: 1oz and 2oz are typically standard, though some PCB manufacturers have a 10-20% increase for going to 2oz. The answer to the second question varied, either specifying that it depends on the design, that it would increase the cost by 25%, or that it would result in a fixed cost increase per panel (e.g. +$25/panel).

E. Board Thickness and Stack-ups

Question: Our understanding is that if standard board thicknesses are used (e.g., 62, 93 mils, 125 mils), the change in cost is relatively low (less than 10%). Would you agree with this?

Summary of responses: There was agreement on this point, and common standard board thicknesses were 31, 62, 93, and 125 mils. These thicknesses are created using standard stack-ups, and a given stack-up is not inherently more costly than others if standard core and prepreg thicknesses are being used. Non-standard stack-ups require direct quotation, and no manufacturers would provide a qualitative cost assessment owing to the open-ended possibilities.

F. Dielectric Material

Manufacturers were asked about their stock options for dielectric materials, and their estimated relative cost difference compared to standard FR-4. The responses received suggest the following cost increases compared to ‘default’ FR-4 for commonly stocked materials: EM-827 (10%), Isola 370HR (25%), Isola FR408HR (25%), Rogers 3000 and 4000 Series (30-60%), and Isola P95 (Polyimide) (25-30%). Manufacturers can source non-stocked materials, but these may be subject to minimum order quantities that may not be feasible for all buyers.

G. Board Milling

All planar magnetic PCBs feature cut-outs for inserting the planar core. Most designs feature three cutouts, though some have four or more. It was generally assessed that cost is weakly affected if more than three slots for the core must be milled.

H. A ‘Qualitative’ Cost Model

One option for developing a planar magnetic winding cost model is to use these qualitative cost impacts as quantitative indices in a model. It is emphasized that these qualitative responses were roughly given for a single variable change (e.g., if everything else is held constant, what is the impact of a variable changing?). Thus, combining these responses to create a cost model is tenuous. However, we proceed in doing this primarily as it is still a useful illustration of the interpretation of the qualitative responses.

Consider defining a sample baseline having 4 layers, only through-hole vias, using stock FR-4, and with 1oz copper thickness on all layers. Then, the effect of a new design which changes these options can be assessed as follows.

Assuming copper weights greater than or equal to 1oz, the cost impact of *increasing* the copper thickness is:

$$\mathrm{CostC} = (1 + \mathrm{ozCost})^{(\mathrm{Oz}-1)} \tag{1}$$

where Oz is the new copper thickness, and ozCost is between 0.1 or 0.2 as per the manufacturer responses. Adding via costs and assuming an increase in via sets of ΔViaSet

$$\mathrm{CostCV} = \mathrm{CostCu} * (1 + \mathrm{ViaSetCost})^{(\Delta\mathrm{ViaSet}-1)} \tag{2}$$

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[3] L1 means “Layer 1”.

[4] 1-3oz copper would be the target for planar magnetics in the 200kHz+ regime.

where ViaSetCost is between 0.2 and 0.3. Adding layer costs and assuming an increase in layer count of ΔLayers

$$\text{CostCVL} = \text{CostCuVia} * (1 + \text{LayerCost})^{\frac{\Delta\text{Layers}}{2}} \tag{3}$$

where LayerCost is between 0.35 and 0.4. Adding dielectric material and board area costs, the resulting cost estimate using these qualitative indices is

$$\text{CostCVLMA} = \text{CostCVL} * \text{AreaIncrease} * (1 + \text{MatCost}) \tag{4}$$

where AreaIncrease indicates the relative change in area (e.g., new board area / old board area), and MatCost is taken from the manufacturer responses.

As an example of using this model, consider a new design which has two via sets, 6 layers, uses 2oz copper, has half the area of the baseline, and uses Isola FR408HR. The estimated cost increase of this new PCB using this 'qualitative' model is:

$$\begin{aligned}\text{New cost} &= (1 + \text{ozCost}) \times (1 + \text{ViaSetCost}) \\ &\quad \times (1 + \text{LayerCost}) \times \text{AreaIncrease} \\ &\quad \times (1 + \text{MatCost})\end{aligned} \tag{5}$$

Using the upper end of the indices from the manufacturer responses (ref. Table I), we find

$$\begin{aligned}\text{New cost} &= (1 + 0.2) \times (1 + 0.3) \\ &\quad \times (1 + 0.4) \times 0.5 \\ &\quad \times (1 + 0.25) = 1.37\end{aligned} \tag{6}$$

The 'prediction' is that this new board is 37% more costly per unit. A reasonable interpretation of this number is that the new design has a low-to-moderate cost impact. To further improve the ability to assess planar magnetic winding cost, one can build a model derived from direct manufacturer-provided data. This approach is discussed in the remainder of this paper.

III. QUANTITATIVE COST DATA

A quantitative cost model must be built on manufacturer-obtained cost data. The central challenge is that it is impractical to obtain data that can encompass all variations of the variables identified in Section 2. So, in this paper we focus on a specific class of planar magnetic component. However, the modeling approach can apply more generally for readers who obtain additional or supplementary data. The idea is that after obtaining a few quotes of interest, one can:

1) Leverage the proposed modeling approach to infer cost impacts of changes to the quoted designs without having to get re-quoted, and/or
2) Add the obtained data to a larger subset of public data (e.g., the data in this paper) in order to create a stronger and more general cost model.

Here, we limit our scope to designs which are able (in principle) to satisfy the medium voltage requirements specified by [6] and which are key to the LCOE optimization in [7], as discussed in the introduction. Doing so improves the cost evaluation in this particularly cost-constrained application. These transformers are bottlenecked by their insulation requirements, and the literature suggests the use of high layer count interleaved builds having non-standard dielectric material (e.g., the uncommon Panasonic RF775 is used in [6]) and using only through-hole vias. We also consider the *possibility* of four layer designs which can satisfy the isolation requirement[5]. The designs are summarized in Table II.

The four layer designs are all built with blind vias between L1-L2 (primary) and L3-L4 (secondary). The spacing between L2-L3 dictates the isolation capability. At higher layer counts, only through hole vias are considered owing to the very high via set cost penalty if more than three via sets is used, but as a result these PCBs must be physically larger to accommodate clearances for the through-hole vias [6]. The quantities are limited to 50 units, which reflects the kinds of quantities a research laboratory or start-up might be reasonably quoted. The special RF775 dielectric is not commonly stocked. Manufacturers 1 and 2 were unable to provide quotes with this material, while manufacturers 3 and 4 were only able to quote up to 10 units. It is emphasized that customers with larger purchasing power will see different costs than what is quoted here[6]. In particular, lower quantities are dominated by fixed costs and the per-unit cost becomes clearer at higher order units. This informs the choice in our model to define fixed and variable cost elements. Explicit fixed costs, such as non-recurring engineering and testing were only quoted by manufacturer 4, reflecting a further difficulty that not all manufacturers respond to quotation requests in the same way. To normalize this impact, we simply added these costs to the total cost. Similarly, we specified that lead time was unimportant to us in order to minimize this additional cost feature impact and took the longest lead time quoted by each manufacturer, but these were different (M1: 10 days, M2: 5 weeks, M3: 11 days, M4: 9 weeks). We did not specify the IPC class (IPC Class 2 is in quotes) and were quoted as Non-ITAR[7].

IV. QUANTITATIVE COST MODEL

As mentioned in Section III, our goal is to showcase a modeling approach which is well-suited for this kind of complex, highly variable PCB data, and which can be built upon by future users with their own relevant data (or who may combine their data with the data presented in this paper in order to build a more general cost model).

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[5] At this stage, we only consider dc withstand capability as done in [6], which is determined by multiplying the de-rated blocking voltage of the dielectric by its thickness [16]. Additional important considerations, such as ac withstand and partial discharge, must still be investigated.

[6] It is further noted that there is a 'human' element to being quoted for a PCB since a person is making a judgement on price. Cost data for the same PCB design is likely to be time-varying even just for this reason. This is another feature of cost which may reveal itself if sufficiently high quantities are ordered, or when a relationship with a manufacturer is developed

[7] ITAR (International Traffic in Arms Regulation) compliance. Non-ITAR means ITAR compliance is not required.

TABLE II: PCB cost data. All quotes use 2oz copper on all layers. Designs 1-6 employ stock FR-4, four layers, two sets of blind vias while designs 8 and 10 use RF775 and only through-hole vias. Designs 7 and 9 are identical to designs 8 and 10, respectively, except they were quoted with FR-4 dielectric (to isolate dielectric cost).

Design	PCB dim.	Spacing	Man. 1 [Q: $ cost]	Man. 2 [Q: $ cost]	Man. 3 [Q: $ cost]	Man. 4 [Q: $ cost]
1	4.57x5.01”	L2-L3: 52 mils	**5:** 4,112.9 **10:** 4,127.3 **20:** 4,714.6 **50:** 6,387.5	**5:** 1,135.0 **10:** 1,582.0 **20:** 2,207.6 **50:** 3,573.5	**5:** 3,450 **10:** 3,580 **20:** 3,875 **50:** 4,765	-
2		L2-L3: 70 mils	**5:** 4,112.9 **10:** 4,127.3 **20:** 4,714.6 **50:** 6,387.5	**5:** 1,145.0 **10:** 1,595.0 **20:** 2,237.6 **50:** 3,648.5	**5:** 3,431 **10:** 3,580 **20:** 3,877 **50:** 4,767	-
3		L2-L3: 96 mils	**5:** 3,434.8 **10:** 3,434.8 **20:** 4,160.6 **50:** 6,116.0	**5:** 1,165.2 **10:** 1,502.3 **20:** 2,172.6 **50:** 3,673.5	**5:** 3,450 **10:** 3,600 **20:** 3,950 **50:** 4,950	-
4	8.62x5.01”	L2-L3: 52 mils	**5:** 4,127.3 **10:** 4,714.5 **20:** 5,844.8 **50:** 9,667.5	**5:** 1,457.3 **10:** 2,082.6 **20:** 2,823.2 **50:** 5,094.5	**5:** 3,565 **10:** 3,850 **20:** 4,400 **50:** 6,150	-
5		L2-L3: 70 mils	**5:** 3,573.3 **10:** 4,160.5 **20:** 5,290.6 **50:** 8,559.5	**5:** 1,472.3 **10:** 2,112.6 **20:** 2,883.2 **50:** 5,229.5	**5:** 3,565 **10:** 3,850 **20:** 4,400 **50:** 6,150	-
6		L2-L3: 96 mils	**5:** 4542.8 **10:** 5,268.5 **20:** 6609.2 **50:** 10,792	**5:** 1,502.3 **10:** 2,172.6 **20:** 3,003.2 **50:** 5,499.5	**5:** 3,600 **10:** 3,900 **20:** 4,500 **50:** 6,400	-
7	4.57x8.71”	10 layers; 5 mil b/w layers	-	-	**5:** 3,579	-
8			-	-	**5:** 19,800	-
9	4.57x8.21”	12 layers; 5 mil b/w layers	-	-	**5:** 4,500	**4:** 3,473 **10:** 4,982
10			-	-	**5:** 23,600	**2:** 26,675 **4:** 39,107 **10:** 69,245

A. Model structure using cost indices

The model assumes that cost impacts can be split into fixed and quantity-dependent (or “variable”) features.

These features are captured by ‘cost indices’ such that total cost (TC) can be computed as

$$\begin{aligned}\mathrm{TC} =&\mathrm{GFC} \times \mathrm{DFI}_d \times \mathrm{MFCI}_m \\ &+ \mathrm{Q} \times (\mathrm{DIVC} + \mathrm{BA} \times \mathrm{DI}_d \times \mathrm{LI}_l \times \mathrm{GVC} \times \mathrm{MVCI}_m)\end{aligned} \tag{7}$$

In this model, there are fixed cost indices related to:

1) General fixed costs (GFC), such as the labor and overhead required to manufacture a PCB separate from the quantity that is produced or the specific design parameters. The model fits a single value of GFC on all of the data it is trained on in an attempt to extract a single “general” fixed cost associated with manufacturing a PCB.
2) Choice of dielectric material (DFI_d). For example, if a material is not typically stocked, then there may be an upfront cost in stocking that material which the customer incurs separate from the number of units that are ordered. Every material that is part of the training data is assigned its own value of DFI (and labeled with a unique numerical subscript d), with DFI_1 assigned to 1. This indicates the relative fixed cost of using a different dielectric.
3) Choice of manufacturer (MFCI_m), which modulates the above costs (e.g. different manufacturers may have different labor or overhead costs, or different ability to source dielectrics). Every manufacturer that is part of the training data is assigned its own value of MFCI (and labeled with a unique numerical subscript m), MFCI_1 assigned to 1. This indicates the relative fixed cost of using a different manufacturer.

There are also costs related to the quantity of PCBs which are being manufactured, which we term “variable costs”. Specifically, we consider:

1) Choice of dielectric material (DI_d). Every material that is part of the training data (labeled with numerical subscript d) is assigned its own value of DI, with DI_1 assigned to 1.
2) Number of layers (LI_l). One LI value is produced for each layer configuration in the data that is being fitted (labeled with numerical subscript l which is equal to the number of layers), with one layer count assigned to 1. For example, if the data has 4, 10, and 12 layer information, then three LI indices are produced which indicates the relative cost of moving between these layer configurations.
3) General variable costs (GVC). The model fits a single value of GVC on all of the data it is trained on in an attempt to extract a single indicator of variable costs that can be impacted by board area. For example, it can capture scrap and copper weight effects.
4) Design-independent variable costs (DIVC), such as the labor and overhead required to manufacture a given PCB design which scale with the number of units that must be produced but are independent of the design details, including board area. In principle this can always be set to zero and its impacts absorbed by GVC, but its inclusion is a reasonable generalization (separating quantity-dependent effects from quantity- and area-dependent effects).
5) The choice of manufacturer (MVCI_m) which modulates the above costs. Each manufacturer is assigned a value of MVCI (labeled with numerical subscript m), with MFCI_1 assigned to 1.

The derivative of TC with quantity is the *marginal cost* (MC) index, which is indicative of the per-unit costs at higher order quantities (i.e., where fixed cost effects have negligible impact on the cost of one additional unit).

$$\mathrm{MC} = \frac{d\mathrm{TC}}{d\mathrm{Q}} = \mathrm{DIVC} + \mathrm{BA} \times \mathrm{DI}_d \times \mathrm{LI}_l \times \mathrm{GVC} \times \mathrm{MVCI}_m \tag{8}$$

The indices of the model can be interpreted as relative cost factors for the feature captured by each index. For example, the quantitative data used in this study contains designs having 4, 10, and 12 layers. We choose four layers to have LI=1, and the fitted model will produce index values for 10 layers and 12 layers (for example, LI_4=1, LI_{10}=2.6, LI_{12}=3.0). This indicates the relative cost penalty of a design changing between these layer counts which is separated from the other index factors. Thus, the cost indices approach has the advantage that cost trends or comparisons of two designs can be made by eliminating the manufacturer's parameter and quantity parameters to compare the cost of designs.

Note that there are no indices for via configuration or copper weight in (7). In the former case, this is because the quotations have a direct coupling between via configuration and layer count – the four layer boards use two sets of blind vias while the higher layer boards use only through hole vias. So, these two features are combined into the layer count. In the latter case, there is only one copper weight to be fit from the data and so the model does not require an index for this parameter. Extending the model to add additional features is discussed in Section IV-C.

To determine the values of the indices in the model, the following optimization procedure is employed

$$\begin{aligned} \min_{\text{indices}} \quad & \frac{1}{N}\Sigma_{i=1}^{N}|\text{Estimate(quote)} - \text{Actual(quote)}|^2 \\ \text{s.t.} \quad & GFC \geq 0,\ DFI_d \geq 0,\ MFCI_m \geq 0, DI_d \geq 0 \\ & LI_l \geq 0,\ GVC \geq 0,\ MVCI_m \geq 0,\ DIVC \geq 0 \\ & LI_4 = MFCI_1 = MVCI_1 = DFI_1 = DI_1 = 1 \end{aligned} \tag{9}$$

where N is the total number of training quotes, Estimate(quote) is the estimated cost of a given PCB design, Actual(quote) is the actual cost of a given PCB design, $d = 1$ is assigned to 'stock' FR-4 provided by each manufacturer, and $d = 2$ is assigned to Felios RF775. The optimization minimizes the mean squared error between the estimated and actual cost within the space of the indices and the stated bounds.

The model is trained on all of the obtained quotes described in Section III and the resulting indices are shown in Table III. The model achieves a 6.53% mean absolute percentage error (MAPE) with standard deviation 4.65% on absolute percentage error between predicted and quoted values on the training set, as shown in Figure 2.

B. Using the Model

To evaluate the predictive power of the model, we obtained new quotes from manufacturers 3 and 4 for a smaller planar transformer design approximately 2 months after obtaining the original data. These designs employ 4 layers, 2oz copper, have dimensions 2.61x5.21", and use blind vias from L1-L2 and L3-L4. We requested quotations for both FR-4 and RF-775 dielectrics. The results for 50 units are summarized in Table IV. The model has excellent predictive power for manufacturer 3 with FR-4, which tracks with the fact that the model was trained on a high quantity of data having this configuration. The prediction from this manufacturer for RF-775 is poor, at 58% error, and this is attributable both to the very low number of training data (only two quotes from this manufacturer for this material) and the fact that this training data was only for 5 units (likely skewing towards assuming higher fixed costs and thus overestimating the 50 unit cost). Estimates predicted from manufacturer 4 are reasonable at 20% and 30% error for FR-4 and RF-775, respectively, demonstrating good predictive power even on a manufacturer that had very limited training data (5 quotes total; one PCB design quoted for two dielectrics). A simple analysis to include panelization suggests that this smaller design has better panel utilization on average than the training data, which should have a tendency to cause our model to over-predict cost.

TABLE III: Cost model indices

Feature/Index	Value
Design-independent / General	
GFC / GVC / DIVC	3304 / 2.72 / 0.0
Dielectric and Layers	
FR-4[8]	DFI_1=DI_1 = 1.0
Felios RF775	DFI_2= 19.3; DI_2 = 4.1
Layers	LI_4=1.0; LI_{10}=2.6; LI_{12}=3.0
Manufacturers	
Manufacturer 1	$MFCI_1$ = 1.00; $MVCI_1$ = 1.00
Manufacturer 2	$MFCI_2$ = 0.32; $MVCI_2$ = 0.75
Manufacturer 3	$MFCI_3$ = 1.04; $MVCI_3$ = 0.34
Manufacturer 4	$MFCI_4$ = 0.75; $MVCI_4$ = 0.99

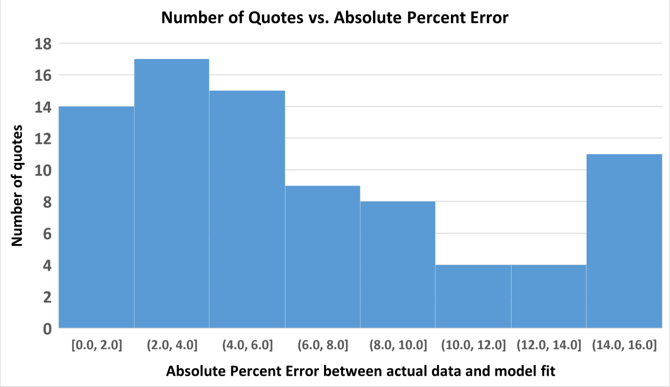

Fig. 2: Summary of the cost index model error on the data it was trained on.

C. Extending the Model

The model can be extended to model other features of interest. For example, the model implementation described above has no index for copper weight since all of the data it was trained on used 2oz copper. To include this, it is ideal to obtain additional data which is only different in terms of the quoted copper weight. A beneficial feature of the model is that this data can in principle be obtained from one manufacturer, simplifying this extension process. For example, we obtained quotations for designs 1 and 3 in Table II having 3/2/2/3 oz copper distribution from Manufacturer 1, which we model as an effective copper index of 2.5 oz. The obtained quotes for

TABLE IV: Model error on new data.

Manufacturer	Material	Actual ($)	Est. ($)	Error
3	FR-4	3610	4065	13%
3	RF775	16335	25870	58%
4	FR-4	6153	4307	30%
4	RF775	37545	45215	20%

design 1 were: 4 units, $4066.4; 12: $4406.5; 48: $6620.2; $96: 8877.1. The obtained quotes for design 3 were: 4 units, $4481.8; 12: $4822; 48: $7137.6; $96: 9930.2.

When adding a new index, a choice must be made on if it should be a fixed index, a variable index, or both. For example, here, we define two new indices: fixed copper cost index (FCuI_c) and variable copper cost index (VCuI_c), where c labels the copper weight. Since the obtained data is identical except for the copper index, the cost relationship of the newly obtained data can be simplified to: Cost = $\mathrm{GFC}_{\mathrm{new}} \times \mathrm{FCuI}_c + \mathrm{Q} \times \mathrm{GVC}_{\mathrm{new}} \times \mathrm{VCuI}_c$. Setting $\mathrm{FCuI}_2 = \mathrm{VCuI}_2 = 1$. We can explore which is more predictive and choose that to be to the index that is used[9], and this is done below:

1) Case 1: Copper weight is only a variable cost: For design 1 alone, this results in $\mathrm{GFC}_{\mathrm{new}} = 3794.79$, $\mathrm{GVC}_{\mathrm{new}} = 50.544$, and $\mathrm{VCuI}_2.5 = 1.07$. The fit gives an average absolute error of 1.95% relative to actual costs. For design 3 alone, the result is $\mathrm{GFC}_{\mathrm{new}}=3298.94$, $\mathrm{GVC}_{\mathrm{new}} = 55.10$, and $\mathrm{VCuI}_2.5 = 1.3$ with an average absolute error of 5.83%. If we use the index values used for design 9 to predict the cost of design 11, we get an error ranging from 14% (Q=50) to 38% (Q=10), suggesting it is well-predictive at higher quantities.

2) Case 2: Copper weight is only a fixed cost: For design 1 alone, this results in $\mathrm{GFC}_{\mathrm{new}} = 3708$, $\mathrm{GVC}_{\mathrm{new}} = 53$, and $\mathrm{FCuI}_2.5 = 1.04$. The fit gives an average absolute error of 1.98% relative to actual costs. For design 3 alone, the result is $\mathrm{GFC}_{\mathrm{new}}=3001$, $\mathrm{GVC}_{\mathrm{new}}=60.5$, and $\mathrm{FCuI}_2.5 = 1.39$ with an average absolute error of 1.99%. If we use the index values used for design 9 to predict the cost of design 11, we get an error ranging from 14% (Q=50) to 33% (Q=10), suggesting it is well-predictive at higher quantities.

The result in both cases is similar, suggesting either or both index choice is valid. Note that accounting for it as a fixed cost element leads to improved error at low quantities, but that the higher-quantity error is the same, which is sensible given the importance of fixed cost at low quantities.

D. Strengths of the Modeling Approach

Other PCB cost modeling approaches focus on information that is harder to get as a customer, such as knowing equipment time and exact costs assigned with each manufacturing process (the “ABC method”) [17] or require knowledge of the detailed material usage in a processes [18]. The reason is likely due to this literature being developed from a manufacturing system analysis perspective, where the focus is on production-side emulation. While such modeling is helpful in understanding or capturing general cost impacts, it does not translate well into a model that can be fit and used to predict or compare designs – the kind of model that planar magnetic winding designers need if they wish to enable cost-informed design or to include planar magnetic costs in LCOE estimates.

Furthermore, the model in this paper is rooted in planar magnetic windings rather than on the more general possibilities of PCB design. This makes a cost model feasible since there is a reduced feature scope. For example, other more-general applications use smaller traces or more vias when they go to a higher number of layers and the number of layers versus area trade-off is more constrained by pin density [19], [20] and other density feature metrics which are unimportant in planar magnetic windings. Similarly, planar windings are unlikely to require the use of microvias and buried vias. Planar magnetic designs have flexibility in the choice of the number of layers and board area without necessarily requiring a need for a technology change (e.g., feature size change). As layer counts increase, a planar magnetic designer may consider employing interleaved over non-interleaved designs, but these are typically also built with through-hole constructions (manufacturing complexity is not introduced by this trade-off) [6], [21].

The model offers an intuitive structure: the indices can be bounded to be positive and can be interpreted as indicating the relative cost importance of a design feature (such as number of layers or dielectric choice). They allow natural extension of the model to new cost elements, and updating specific indices over time. Furthermore, the limits of the model are explicit, since an index is provided for every multi-variable feature the model was trained on. While the model is capable of inferring cost from design combinations it was not trained on, it is also explicit that the result is being predicted outside of the bounds of the model.

The ability for the model to infer marginal costs is also helpful for designers who are interested in higher volume relationships or in comparing with something that is already in market. For example, LCOE analysis compares to a benchmark product which is likely to be at high volume, but it is difficult for researchers to assess high volume cost directly. Separation of the model structure into fixed and variable elements enables representative per-unit cost trends to be elucidated from quotations at relatively low volumes, improving the feasibility of this kind of estimation.

E. Model Limitations and Future Work

A key limitation of the model is that it does not have strong predictive power for design elements that were not in the trained data or which cannot be inferred from the data. For example, via configuration is connected to dielectric material in the data we obtained, so the model does not distinguish these features and a new combination of these features is poorly predicted. Another important limitation for future work is that the cost model does not account for panelization. The impact of board area translates into cost according to how many panels are used, and this is a function of the dimensions

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[9] Both indices can always be used, but the added complexity may not be justified by improved predictive power.

of the PCB rather than just its area. This is an especially important aspect to include since a design which is optimized to maximize the available panel area is likely to be less costly than one that does not, even if their areas are the same [17].

V. CONCLUSION

Planar magnetics are being actively pursued in a wide range of power electronics applications, with their low cost being a key driver. However, their costs do not scale clearly with volume owing to a strong dependence on manufacturing complexity. While existing work identifies the general trends of their costs (e.g., simpler boards are generally less costly), there is no aggregated basis for a quantitative assessment. This paper addresses this challenge. First, a qualitative summary of cost impacts is presented. Then, a quantitative cost model structure is proposed and evaluated. This model is built on intuitive cost indices which can be assigned to key cost features such as layer count, dielectric material, and copper width, and which can be computed from cost data from multiple PCB designs and manufacturers. The model can be integrated into existing optimization procedures to better capture the cost impact of using planar magnetic windings, which are currently not well-modeled or not included in cost models. For example, it can improve existing work on LCOE optimizations employing planar transformers. Strengths, weaknesses, and future extensions of the model are discussed. The developed model has good predictive power on designs that are well-represented by data it was trained on (13% error), and within 20-58% error on designs which have limited representation in the training data.

REFERENCES

[1] Z. Ouyang and M. A. E. Andersen, "Overview of planar magnetic technology—fundamental properties," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014.

[2] M. K. Ranjram and D. J. Perreault, "A 380-12 v, 1-kw, 1-mhz converter using a miniaturized split-phase, fractional-turn planar transformer," *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1666–1681, 2022.

[3] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, "Novel techniques to suppress the common-mode emi noise caused by transformer parasitic capacitances in dc–dc converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4968–4977, 2013.

[4] D. Huang, S. Ji, and F. C. Lee, "Llc resonant converter with matrix transformer," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4339–4347, Aug 2014.

[5] Z. Zhou, Y. Gao, X. Zhang, and H. Ma, "A design principle ensuring uniform flux density distribution of the two middle legs planar core for llc converter," in *2022 IEEE 1st Industrial Electronics Society Annual On-Line Conference (ONCON)*, Dec 2022, pp. 1–5.

[6] S. Mukherjee, B. Majmunovic, G.-S. Seo, S. Dutta, R. Mallik, B. Johnson, and D. Maksimović, "A High-Frequency Planar Transformer with Medium-Voltage Isolation," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*. Phoenix, AZ, USA: IEEE, Jun. 2021, pp. 2065–2070.

[7] G.-S. Seo, S. Mukherjee, J. Roy, K. Goodrick, R. Mallik, B. Majmunovic, S. Dutta, D. Maksimović, and B. Johnson, "Levelized-cost-of-electricity-driven design optimization for medium-voltage transformerless photovoltaic converters," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6973–6980.

[8] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, T. McNutt, and A. B. Lostetter, "High-frequency ac-dc conversion with a silicon carbide power module to achieve high-efficiency and greatly improved power density," in *2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, July 2013, pp. 1–5.

[9] M. H. Ahmed, A. Nabih, F. C. Lee, and Q. Li, "High-efficiency, high-density isolated/regulated 48v bus converter with a novel planar magnetic structure," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 468–475.

[10] B. Whitaker, Z. Cole, B. Passmore, D. Martin, T. McNutt, A. Lostetter, M. N. Ericson, S. S. Frank, C. L. Britton, L. D. Marlino, A. Mantooth, M. Francis, R. Lamichhane, P. Shepherd, and M. Glover, "High-temperature sic power module with integrated sic gate drivers for future high-density power electronics applications," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, Oct 2014, pp. 36–40.

[11] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[12] A. Maswood and L. K. Song, "Design aspects of planar and conventional SMPS transformer: a cost benefit analysis," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 3, pp. 571–577, Jun. 2003.

[13] L. H. Dixon, "How to design a tranformer with fractional turns," in *Unitrode/TI Magnetics Design Handbook*, no. Topic R6, TI Literature Number: SLUP132, 2000.

[14] R. P. Hedden, *Cost engineering in printed circuit board manufacturing*, ser. Cost engineering. New York: M. Dekker, 1987, no. 11.

[15] C. Sullivan, "Cost-constrained selection of strand diameter and number in a Litz-wire transformer winding," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting*, vol. 2, Oct. 1998, pp. 900–906 vol.2, iSSN: 0197-2618.

[16] R. Tarzwell and K. Bahl, "High Voltage Printed Circuit Design & Manufacturing Notebook."

[17] R. E. Giachetti and J. Arango, "A design-centric activity-based cost estimation model for pcb fabrication," *Concurrent Engineering*, vol. 11, no. 2, pp. 139–149, 2003. [Online]. Available: https://doi.org/10.1177/1063293X03035372

[18] P. Sandborn and C. Murphy, "Material-centric modeling of pwb fabrication: an economic and environmental comparison of conventional and photovia board fabrication processes," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part C*, vol. 21, no. 2, pp. 97–110, 1998.

[19] T. Chiba, M. Yamada, and F. Kobayashi, "Limitation of the signal pin density on wiring boards," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 19, no. 2, pp. 391–396, May 1996.

[20] "How to Determine the Number of Layers in PCBs — PCBCart — pcbcart.com," https://www.pcbcart.com/article/content/factors-determining-PCB-layers.html, [Accessed 15-Jun-2023].

[21] M. K. Ranjram *et al.*, "Design considerations for planar magnetic terminations," in *20th Workshop on Control and Modeling for Power Electron. (COMPEL)*, June 2019, pp. 1–8.