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Reverse Leakage Analysis for As-Grown and Regrown Vertical GaN-on-GaN Schottky Barrier Diodes

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ABSTRACT Vertical GaN-on-GaN Schottky barrier diodes based on as-grown and regrown samples were fabricated to investigate the effects of the etch-then-regrow process on device performance. The surface roughness increased slightly after dry etching and decreased after regrowth. According to X-ray diffraction results, the etch-then-regrow process caused a slight increase of defect density due to increased edge dislocations. Schottky parameters extracted from forward current-voltage curves, such as turn-on voltages of 0.74 V and 0.72 V, ideality factors of 1.07 and 1.10, and barrier heights of 1.07 eV and 1.05 eV, were obtained for diodes based on the regrown and as-grown samples, respectively. The breakdown voltage of the regrown sample was much lower than the as-grown sample. The regrowth interface can be regarded as a n-doping GaN layer due to the high interface charge density after the etch-then-regrown process. This equivalent *n*-doping GaN layer reduced the effective thickness of the UID-GaN under the Schottky contact thus causing lower breakdown voltage for the regrown sample. Poole-Frenkel emission and trap-assisted tunneling processes were responsible for the leakage of both as-grown and regrown samples according to the temperature dependence of the reverse currents.

INDEX TERMS Schottky barrier diodes, GaN-on-GaN, regrow, leakage, interface.

I. INTRODUCTION

Gallium nitride (GaN) has become one of the most important materials for power electronics, due to its superior physical and electrical properties such as large bandgap, high breakdown electric field, high operation temperature and high electron velocity. These characteristics make GaN-based devices capable of remarkable improvements in energy conversion efficiency, increased switching frequency, and reduced electric system volume [1], [2]. Furthermore, as GaN substrates are becoming commercially available, vertical devices grown on GaN substrates have emerged as highly promising candidates for high-performance power electronics due to dramatically reduced density of dislocations [3]–[7].

Meanwhile, in order to achieve the best performance and flexibility in device structure design, selective-area doping is indispensable. Compared with ion implantation [8], [9] and diffusion [10], selective epitaxial regrowth is still the most effective ways for GaN devices. A lot of work on regrown n^+-GaN have been reported that the contact resistance could be dramatically reduced [11]–[13]. Regrown AlGaN/GaN layers was reported to suppress the dispersion of GaN vertical transistors [14].

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However, one big challenge for the regrowth is the interface contamination, including Si, O, and C [15]–[18]. The C and O contaminants could be effectively reduced by *in situ* thermal cleaning [16]. But the Si contamination is difficult to remove even after using Fe or C doping for the semi-insulating substrate or buffer layer [16], [19]–[21], and the origin is still unclear. Although the semi-insulating substrate or buffer layer is useful for reducing leakage current, no leakage performance above 60 V was found in the reported results [16], [19]-[21]. The existence of Si at the interface may not be a problem for the regrown n^+-GaN as ohmic contacts because the Si is the very donor used for *n*-doping. But this is a big problem for the regrowth of *p*-GaN. Hu *et al.* investigated the performance of vertical GaN *p-n* diodes with regrown *p*-GaN, reaching breakdown voltage of 1.1 kV [22]. However, they did the regrowth on a non-etched surface whereas dry etching is almost inevitable in selective regrowth. Recently, Pickrell *et al.* found that regrown diodes including dry etching process prior to the *p*-GaN regrowth showed a large Si spike at the regrowth interface and demonstrated significantly higher reverse leakage current than the as-grown diodes [23]. However, they only showed simple current-voltage curves for the etch-then-regrow diodes. Few reports were found on the details of the effects of the etch-then-regrow process for now. Meanwhile, the co-doping or interaction effect of donors (Si) and acceptors (Mg) could make the interface issue more complex [24]–[26].

To simplify the question and get a direct understanding of the interface issues after the etch-then-grow process, we did the etch-then-grow process by regrowing unintentionally doped (UID) GaN on UID-GaN in this work without the influences of the co-doping or interaction effect of donors and acceptors. In addition to the influences of the etch-then-regrow process on material properties, vertical GaN-on-GaN Schottky barrier diodes were fabricated on both as-grown and regrown samples to investigate the effect of the regrowth interface on device leakage and breakdown.

II. EXPERIMENTAL DETAILS

Both the as-grown and regrown samples were homoepitaxially grown by metalorganic chemical vapor deposition (MOCVD) on 2-inch *c*-plane n^+-GaN (1×10^{18} cm^{-3}) free-standing substrates which were grown by hydride vapor phase epitaxy (HVPE). 2-μm-thick UID-GaN epilayers were first grown on the GaN substrates for both samples. The UID-GaN for the regrown sample was first etched off 500 nm by the inductively coupled plasma (ICP) etching. Then, another 500-nm-thick UID-GaN was regrown on the etched surface using the same growth condition with the original 2-μm-thick UID-GaN without any other surface treatment. The etch-then-regrow process is shown in Fig. 1. Surface roughnesses, measured by atomic force microscopy (AFM), of the as-grown sample, the sample after etching, and the sample after regrowth, are 0.157 nm, 0.207 nm and 0.137 nm, respectively. This means

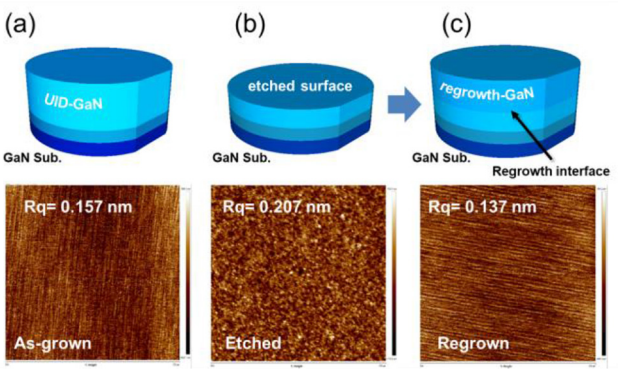

FIGURE 1. Schematics of (a) as-grown sample, (b) sample after etching, and (c) sample after regrowth. The AFM images below compare surface morphology with a scanning area of 5 μm × 5μm.

the surface roughness increased slightly after dry etching but was recovered after the regrowth. The increased surface roughness after dry etching also indicates that etching damage could be introduced by the process. Although the etching damage and corresponding surface roughness can be reduced by optimizing the etching condition, the purpose of this work is to investigate the effect of the dry etching damage on the device performance.

Vertical GaN-on-GaN Schottky barrier diodes (SBDs) based on the as-grown and regrown samples were fabricated by an identical process. Ni/Pt/Au (10 nm/30 nm/120 nm) metal stacks were deposited by electron-beam evaporation for Schottky contacts with a diameter of 120 μm. Mesa isolation, with a diameter of 180 μm and etch depth of 1.5 μm, was done by chlorine-based ICP etching. Metal stacks of Ti/Al/Ni/Au (20 nm/130 nm/50 nm/50 nm) were deposited for ohmic contacts on the backside of the GaN substrate. Forward current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics were measured using a Keithley 4200-SCS parameter analyzer and reverse *I-V* characteristics were measured by a Keithley 2410 sourcemeter.

III. RESULTS AND DISCUSSION

A. DISLOCATIONS

Fig. 2(a) and 2(c) show X-ray diffraction (XRD) omega rocking curves for symmetric (002) and asymmetric (102) reflections, respectively. The full-width-half-maximum (FWHM) for the (002) and (102) reflections are summarized in Figs. 2(b) and 2(d), respectively. The FWHM of the (002) reflection for the regrown sample is almost the same as the as-grown sample. On the other hand, an increase of the FWHM for the (102) reflection after the etch-then-regrow process is obvious (Fig. 2(d)). The results indicate that the etch-then-regrow process mostly influenced edge dislocations because the FWHM for (002) and (102) reflections are typically related to screw and edge threading dislocations, respectively. Similar results on the increase of the FWHM for the (102) reflection were also found in the regrown *p*-GaN after the etch-then-regrow process [17]. Dislocation densities for the as-grown sample, the sample after etching, and the

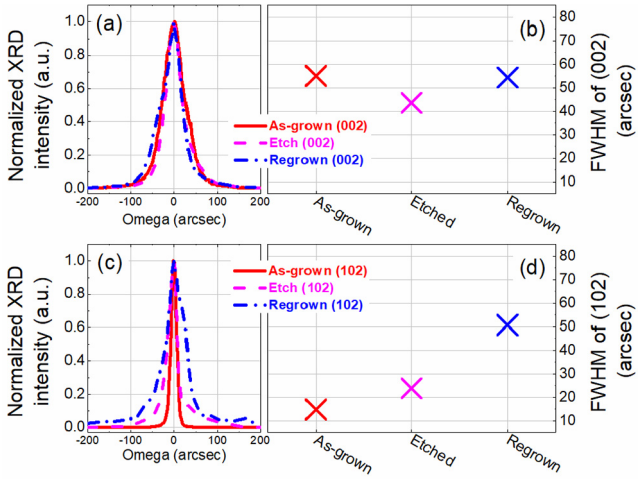

FIGURE 2. (a) XRD omega rocking curves of (002) reflection of as-grown (red line), etched (pink dash) and regrown samples (blue dash dot), and (b) corresponding FWHM. (c) XRD omega rocking curves of (102) reflections, and (d) corresponding FWHM.

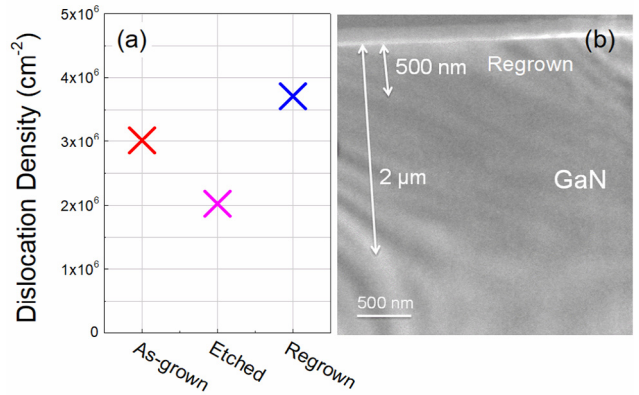

FIGURE 3. (a) Dislocation densities according to XRD. (b) TEM image of the regrown sample.

sample after regrowth are shown in Fig. 3(a). The dislocation densities are all in the range of 10^6 cm^{-3} with a slight increase after the etch-then-regrow process. However, no clear regrowth interface was visible by transmission electron microscopy (TEM) in this work (Fig. 3(b)). This is quite different from the regrown *p*-GaN after the etch-then-regrow process where an interfacial layer at the regrowth interface was clearly observed [17]. Further work is being done to find the reason.

B. FORWARD CHARACTERISTICS

Fig. 4(a) shows the forward *I-V* characteristics for both samples. Turn-on voltages for the as-grown and regrown samples, extracted by linear extrapolation, are 0.74 V and 0.72 V, respectively.

The current equation for forward *I-V* characteristics with $V > 3kT$ can be written as [27]

$$J = J_0 \exp\left(\frac{qV}{nkT}\right) \quad (1)$$

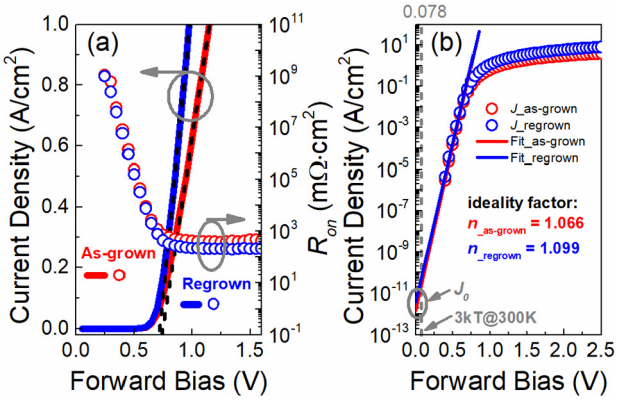

FIGURE 4. (a) Current density in linear scale, and on-resistance in logarithmic scale for as-grown (red), and regrown (blue) samples, as a function of forward bias. Short dash lines indicate turn-on voltages by linear extrapolation. (b) Current density vs. forward bias with semi-log scale. Ideality factor and saturation current density were extracted from linear segments.

where $J_0 = A^{**}T^2 \exp(-q\phi_B/kT)$ is the saturation current density, which can be obtained by extrapolating the current density from the semi-log plot to $V = 0$ V. n is the ideality factor which is related to the slope. A^{**} is the effective Richardson constant, which is theoretically 26.4 A/cm^2/K^2 for GaN [28]. As shown in Fig. 4(b), the ideality factor, and the extrapolated saturation current density, for the device on the as-grown sample are 1.07 and 1.5×10^{-12} A/cm^{-2}, respectively. For the regrown sample, the ideality factor and the saturation current density are 1.10 and 3.8×10^{-12} A/cm^{-2}, respectively. The extracted Schottky barrier heights, ϕ_B, for the as-grown and regrown samples, are 1.07 eV and 1.05 eV, respectively. Thus, Schottky barrier diodes on both samples show quite similar forward characteristics.

C. BREAKDOWN

The reverse *I–V* characteristics of the samples are shown in Fig. 5. The breakdown voltages of the as-grown and regrown samples were 282 V and 89 V, respectively. The breakdown was not due to avalanche for both samples since the breakdown voltage did not increase with the temperature. To investigate the influences of the regrowth interface on the breakdown voltage, charge density profiles of the as-grown and regrown samples were extracted from *C-V* curves at different frequencies (Fig. 6). The charge density of the UID-GaN for the as-grown sample is in the range of $10^{14} - 10^{16}$ cm^{-3}. For the regrown sample, the charge density shows a spike up to 10^{19} cm^{-3} at the depth of $\sim$ 500 nm, where is exactly the location of the regrowth interface. The high charge density is believed to be attributed to the donor-like contaminants, such as Si and O [15]–[18].

To further reveal the effects of the regrowth interface on the device performance, we did device simulation using Silvaco. Based on the discussion above, the regrowth interface was treated as a *n*-doping GaN layer in the simulation. The thickness of the interfacial layer is set to

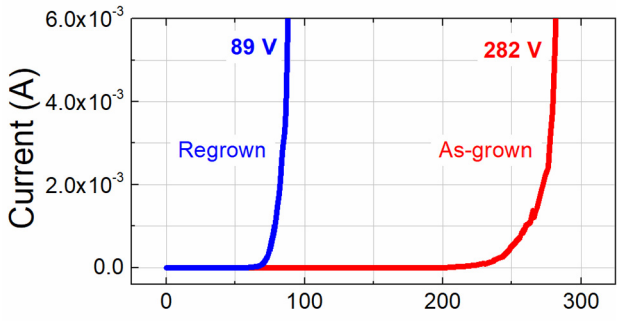

FIGURE 5. Reverse *I-V* curves of Schottky barrier diodes on as-grown (red line), and regrown (blue line) samples.

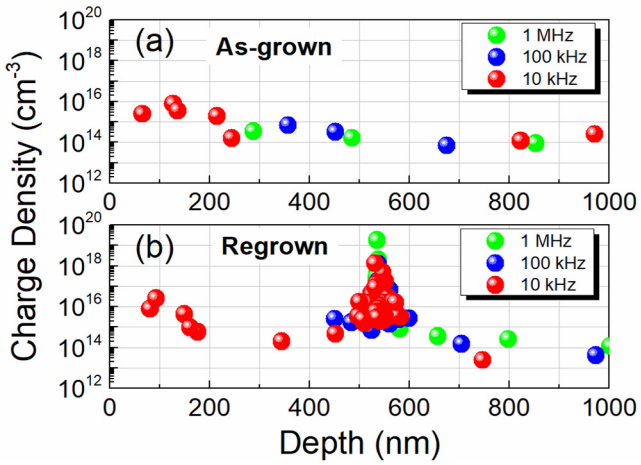

FIGURE 6. Charge density profiles of (a) as-grown sample, and (b) regrown sample extracted from *C-V* results at different frequencies.

100 nm, which is estimated from the charge density profile and secondary-ion mass spectrometry (SIMS). However, the thickness of the interfacial layer is not so important in this simulation. The simulated reverse *I-V* curves are shown in Fig. 7. The regrown sample shows a significantly lower breakdown voltage, which agrees well with the experimental results. Because the simulation did not take the electric field crowing effects around the mesa edges of the diodes into consideration, there are differences in the absolute values of the breakdown voltages between the experimental results and simulation. Figure 7(b) presents the simulated electric field distribution in the samples. For the regrown sample, the reverse bias drops mainly on the regrown UID-GaN (500 nm), whereas the reverse bias drops on the entire UID-GaN (2 µm) for the as-grown sample. Because the effective thickness of the UID-GaN under the Schottky contact for the regrown sample under reverse bias is reduced by the regrowth interface charge, the regrown sample shows a much lower breakdown voltage than the as-grown sample.

D. REVERSE LEAKAGE MECHANISM

To investigate the reverse leakage mechanisms, temperature dependence of reverse *I-V* curves for both samples were measured, as shown in Fig. 8. There are three main

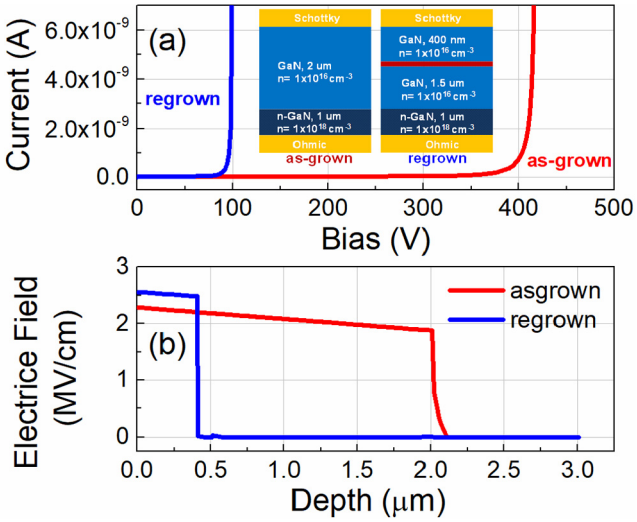

FIGURE 7. Simulations of (a) reverse *I-V*, and (b) electric field distribution at breakdown voltage, for as-grown (red) and regrown (blue) samples. The structures used for simulation are shown in the inset.

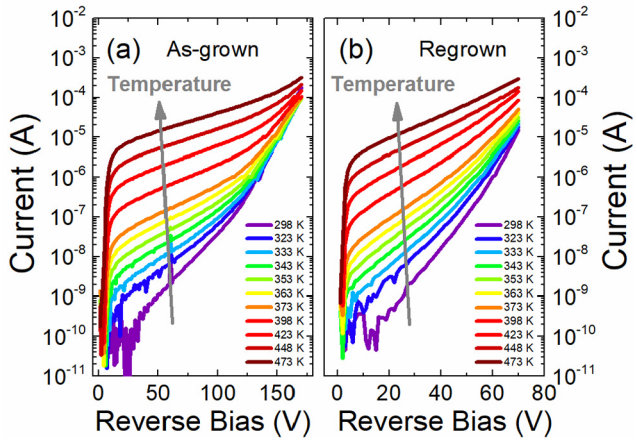

FIGURE 8. Reverse *I–V* characteristics of GaN Schottky barrier diodes at various temperatures on the as-grown sample (a), and the regrown sample (b). Temperature ranges from 298 K to 473 K.

mechanisms responsible for the leakage of Schottky barrier diodes, i.e., thermionic emission (TE) over the barrier, field emission (FE) and thermionic-field emission (TFE) [27]. Furthermore, traps also play an important role in the leakage for GaN-based devices since the dislocation density is still high even for the GaN-on-GaN material. There are several trap-related reverse leakage mechanisms including Poole-Frenkel emission (PFE) [27], variable range hopping (VRH) [29], [30], exponential-tails-trap space-charge-limited current (ETT-SCLC) [31], [32], and trap-assisted tunneling (TAT) [33], [34]. Besides, Fowler–Nordheim tunneling (FNT) [27] is also common observed in dielectrics and wide bandgap semiconductors. The surface leakage is negligible because we found that the reverse leakage current was linearly proportional to the area but not to the perimeter. Possible leakage processes for GaN devices, including the trap-related leakage, are summarized in Table 1 and Fig. 9.

TABLE 1. Leakage Processes and the Expressions

Process	Expression
Thermionic emission (TE) [27]	$J = A^{**}T^2 \exp(\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_s})}{kT}) \times(\exp(\frac{qV}{kT})-1)$
Field emission (FE) [27]	$J = A^{**}(\frac{E_{00}}{k})^2(\frac{\phi_B+V}{\phi_B})\exp(\frac{-2q\phi_B^{3/2}}{3E_{00}\sqrt{\phi_B+V}})$ $E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{m^*\varepsilon_s}}$
Thermionic-Field emission (TFE) [27]	$J = \frac{A^{**}T}{k}\sqrt{\pi E_{00}q[V+\frac{\phi_B}{\cosh^2(E_{00}/kT)}]} \times\exp(\frac{-q\phi_B}{E_{00}\coth(E_{00}/kT)})\exp(\frac{qV}{\varepsilon'})$ $\varepsilon' = \frac{E_{00}}{(E_{00}/kT)-\tanh(E_{00}/kT)}$
Fowler–Nordheim tunneling (FNT) [27]	$J \propto E^2\exp(\frac{-4\sqrt{2qm^*}\phi_B^{3/2}}{3\hbar E})$
Poole-Frenkel emission (PFE) [27]	$J \propto E\exp(\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_s})}{kT})$
Variable range hopping (VRH) [29], [30]	$J \propto \exp(-(\frac{T_c}{T})^{\nu})$
Exponential-tails-trap space-charge-limited current (ETT-SCLC) [31], [32]	$J = q^{1-l}\mu_n N_c(\frac{\varepsilon_s l}{N_t(l+1)})^l(\frac{2l+1}{l+1})^{l+1}\frac{V^{l+1}}{d^{2l+1}}$
Trap-assisted tunneling (TAT) [33], [34]	$J \propto \exp(\frac{-4\sqrt{2qm^*}\phi_t^{3/2}}{3\hbar E})$

A^{**} = effective Richardson constant; ϕ_B = barrier height; ϕ_t = trap energy level; E = electric field; ε_s = static or high frequency dielectric constant (for PFE process); k = Boltzmann constant; T_c = characteristic temperature; ν = 1/2, 1/3, and 1/4 for 1D, 2D, and 3D system, respectively; q = electron charge; μ_n = electron mobility; N_C = effect tive density of conduction band states; N_t = total trap density; d = thickness; $l = kT_c/kT$, kT_c = characteristic energy measured from the transport level; m^* = effective mass; $\hbar$ = reduced Planck constant.

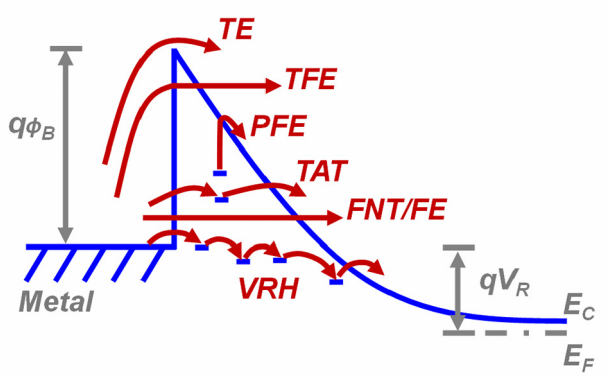

FIGURE 9. Schematic of possible leakage processes under reverse bias for GaN Schottky barrier diodes.

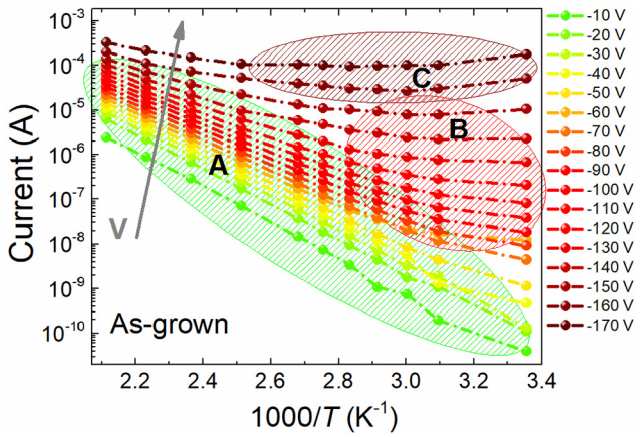

FIGURE 10. Current vs. temperature for the as-grown sample at different voltages.

Leakage due to the TE process is small and negligible here since the barrier height is very high (~1 eV) at reverse bias condition according to the expression shown in Table 1.

According to Fig. 8, the current as a function of $1/T$ for the as-grown sample is plotted in Fig. 10. Three regions with different characteristics are identified (Fig. 10), which are marked as "A", "B" and "C". For the region "A" of the as-grown sample, in the low reverse bias range, the log$I$ follows a linear relationship with $1/T$. This characteristic corresponds to the PFE leakage process, according to the expressions in Table 1. Thus, we can use the linear fitting of the $I - 1/kT$ in semi-log scale to extract parameters for the PFE process (Fig. 11). It is found that the trap level for the PFE process is located at 0.89 eV below the conduction band edge (CBE), and the relative high frequency dielectric constant of GaN, $\varepsilon_r = 5.56$, which is close to the reported values [35]–[37]. The value of the dielectric constant is an important parameter to measure whether the fitting is self-consistent and consistent with the physical process, excluding the situation that it is only a mathematically good fitting.

For the region "B" of the as-grown sample, in the higher reverse bias and low temperature range, the current shows almost flat characteristics with the $1/T$. This behavior could be related to the contributions of tunneling processes (FE, FNT or TAT), TFE, or VRH. Because the log$I$ is still proportional to $1/T$ in the high temperature range for curves in the region "B" which is adjacent to the region "A" where the PFE process dominates, the PFE process also contributes partly to the leakage in the region "B". To better identify the leakage mechanisms at this region, the part of the leakage contributed by the PFE process was subtracted from the total leakage current in the region "B", as shown in Fig. 12(a). The remaining leakage current shows a very weak dependence on the temperature (Fig. 12(b)), indicating a tunneling dominated process rather than the VRH. For the FE process, E_{00} is only 0.4 meV ($N = 1 \times 10^{15}$ cm^{-3},

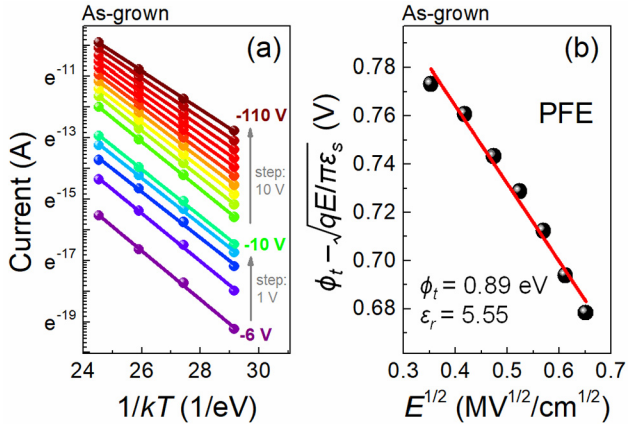

FIGURE 11. (a) Linear fitting of I-$1/kT$ using the PFE model for region "A" of the as-grown sample. (b) Parameters extraction for the PFE model for region "A" of the as-grown sample.

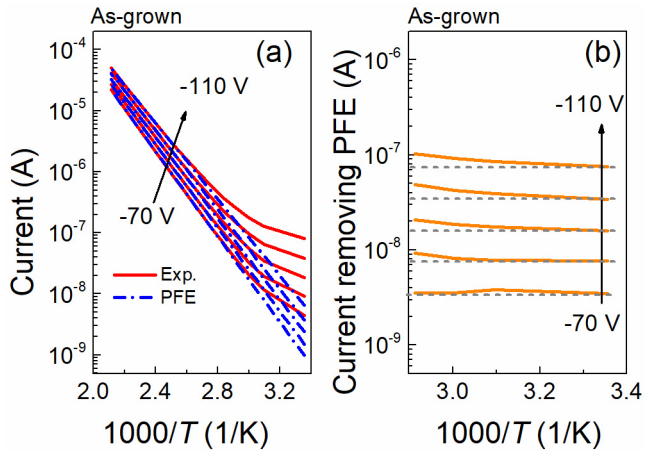

FIGURE 12. (a) Comparison of reverse current at region "B" and the PFE part of the as-grown sample. (b) Current after removal of the PFE part for region "B" of the as-grown sample.

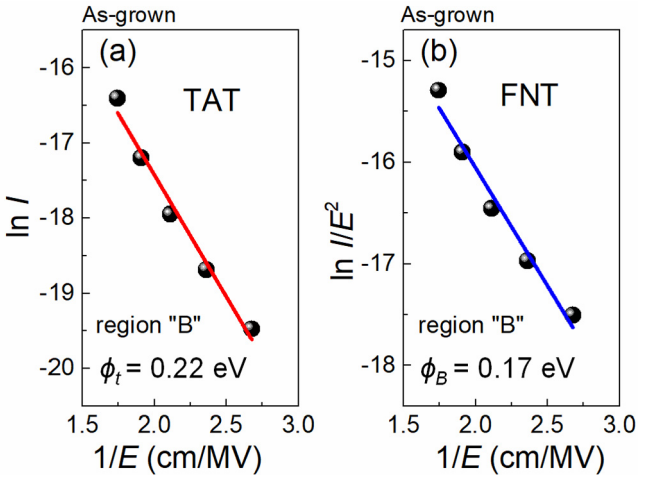

FIGURE 13. (a) TAT plot, and (b) FNT plot, for region "B" ranging from −70 V to −110 V of the as-grown sample.

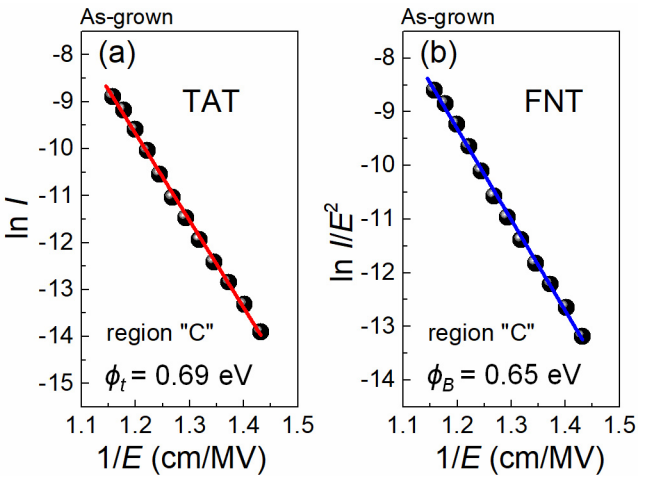

FIGURE 14. (a) TAT plot, and (b) FNT plot, for region "C" ranging from −130 V to −170 V of the as-grown sample.

$m^* = 0.22\ m_e, \varepsilon_{r\_static} = 9.5$). Thus, the leakage current due to the FE is negligible according to the expression in Table 1 [27]. Because both the TE and FE processes are negligible, the TFE process as an intermediate stage of the two processes does not play an important role, either. Linear fitting plots based on the possible TAT and FNT processes as a function of 1/E are shown in Figs. 13(a) and 13(b), respectively. The FNT process, across the Schottky barrier height (1.07 eV), can also be excluded or may contribute to a very small portion of leakage current because the extracted barrier height is only 0.17 eV which is much smaller than the Schottky barrier height. In fact, the FE and FNT are the same here when the device is under large reverse bias. Therefore, the TAT process, with a trap energy level of 0.22 eV, is the dominant mechanism for the leakage in the region "B" of the as-grown sample.

For the region "C" of the as-grown sample, in the high reverse bias range, the leakage current shows a very weak temperature dependence. This characteristic indicates a tunneling process. As shown in Fig. 14, both possible TAT and FNT processes were used to fit the curves of log$I$ vs. 1/E. However, the extracted barrier height for the FNT process is only 0.65 eV which is much smaller than the Schottky barrier height. This means that the FNT model only mathematically fits well with the experimental data. From a physical point of view, the fitting is not self-consistent. So, the FNT process can be excluded or may contribute to a very small portion of the leakage current even though the electric field is very high that is likely to cause the FNT process. Therefore, FNT is not the dominant leakage mechanism. The TAT process, with a trap energy level of 0.69 eV below the CBE, is the dominant mechanism for the leakage in region "C" of the as-grown sample.

The same analysis was done for the regrown sample, as shown in the Figs. 15, 16, 17, 18 and 19. For the region "A" of the regrown sample, the PFE is the dominant process

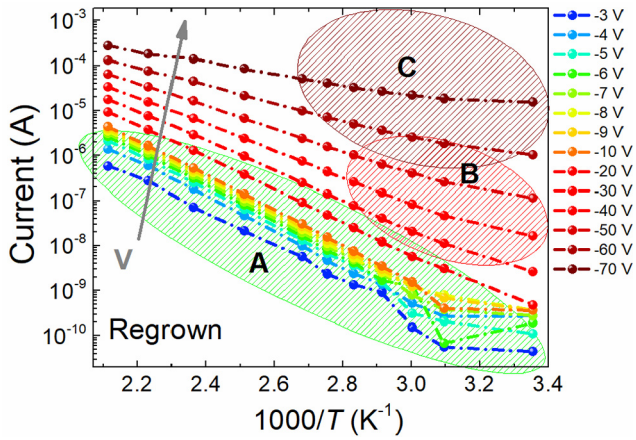

FIGURE 15. Current vs. temperature for the regrown sample at different voltages.

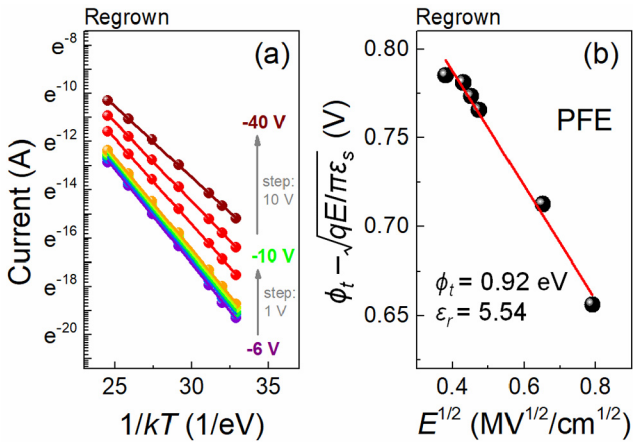

FIGURE 16. (a) Linear fitting of I-1/kT using the PFE model for region "A" of the regrown sample. (b) Parameters extraction for the PFE model for region "A" of the regrown sample.

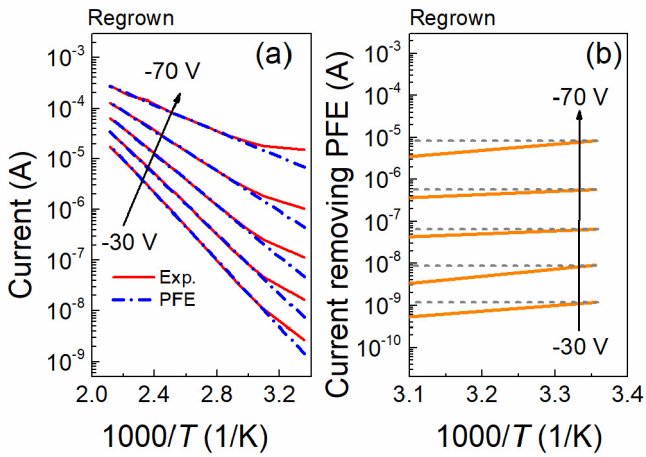

FIGURE 17. (a) Comparison of reverse current at region "B" and the PFE part of the regrown sample. (b) Current after removal of the PFE part for region "B" of the regrown sample.

with a trap energy level of 0.92 eV below the CBE. For the region "B" of the regrown sample, the TAT is the dominant process with a trap energy level of 0.34 eV below the

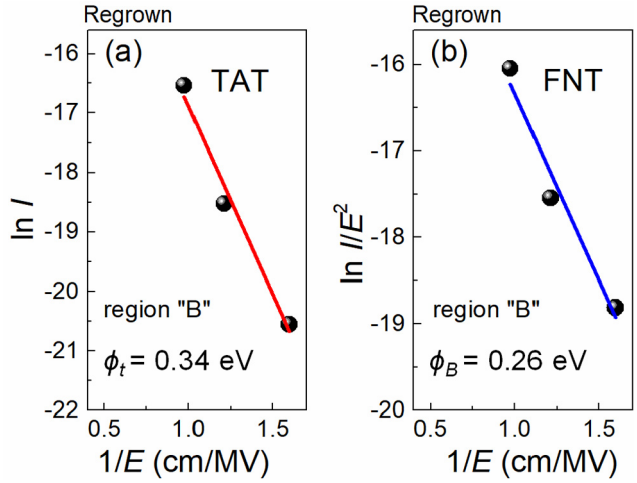

FIGURE 18. (a) TAT plot, and (b) FNT plot, for region "B" ranging from −30 V to −50 V of the regrown sample.

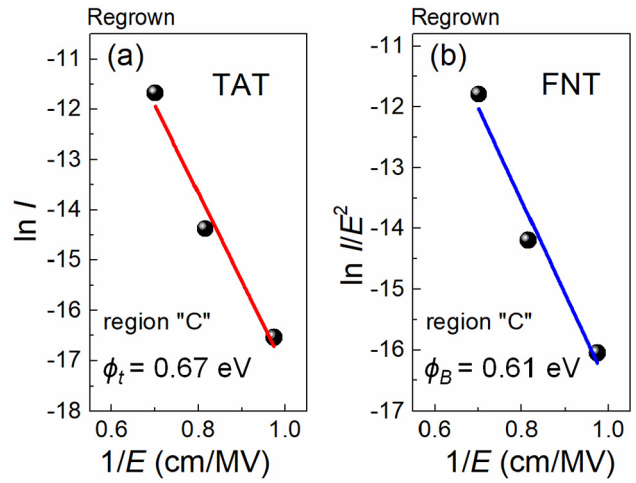

FIGURE 19. (a) TAT plot, and (b) FNT plot, for region "C" ranging from −50 V to −70 V of the regrown sample.

CBE. For the region "C" of the regrown sample, the TAT is also the dominant process with a trap energy level of 0.67 eV below the CBE. Considering all the results above and fitting errors, the same transport processes with quite similar trap energy levels caused the reverse leakage currents for both as-grown and regrown samples. This result agrees well with the previous model that the regrowth interface was regarded as a n-doping GaN layer. This equivalent n-doping GaN layer reduced the effective thickness of the UID-GaN under the Schottky contact. However, because the regrown UID-GaN after the etch-then-regrow process had similar surface morphology and film quality with the as-grown UID-GaN, the Schottky barrier diodes on both regrown and as-grown samples showed quite similar forward I-V curves and the same transport processes for the reverse leakage. Besides, the extracted trap energy levels in this work are close to the reported values in GaN by deep-level transient spectroscopy [38].

IV. CONCLUSION

The influences of the etch-then-regrow process on material properties have been investigated by regrowing UID-GaN on UID-GaN on GaN substrates. Vertical GaN-on-GaN Schottky barrier diodes were fabricated on both as-grown and regrown samples to investigate the effect of the regrowth interface on forward and reverse *I-V* characteristics. Because the regrown UID-GaN after the etch-then-regrow process had similar surface morphology and film quality with the as-grown UID-GaN, the Schottky barrier diodes on both regrown and as-grown samples showed quite similar forward *I-V* curves and the same transport processes (PFE and TAT) for the reverse leakage. It is found that regrowth interface can be regarded as a *n*-doping GaN layer due to the high interface charge density after the etch-then-regrow process. This equivalent *n*-doping GaN layer reduces the effective thickness of the UID-GaN under the Schottky contact thus causing a lower breakdown voltage for the regrown sample.

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REFERENCES

[1] T. Kachi, "Recent progress of GaN power devices for automotive applications," *Jpn. J. Appl. Phys.*, vol. 53, Sep. 2014, Art. no. 100210, doi: 10.7567/jjap.53.100210.

[2] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron. Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[3] I. C. Kizilyalli, P. Bui-Quang, D. Disney, H. Bhatia, and O. Aktas, "Reliability studies of vertical GaN devices based on bulk GaN substrates," *Microelectron. Rel.*, vol. 55, nos. 9–10, pp. 1654–1661, Aug./Sep. 2015, doi: 10.1016/j.microrel.2015.07.012.

[4] I. C. Kizilyalli, T. Prunty, and O. Aktas, "4-kV and 2.8-mΩ-cm^2 vertical GaN $p-n$ diodes with low leakage currents," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1073–1075, Oct. 2015, doi: 10.1109/LED.2015.2474817.

[5] M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-performance GaN vertical fin power transistors on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, Apr. 2017, doi: 10.1109/LED.2017.2670925.

[6] H. Fu *et al.*, "High performance vertical GaN-on-GaN $p-n$ power diodes with hydrogen-plasma-based edge termination," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1018–1021, Jul. 2018, doi: 10.1109/led.2018.2837625.

[7] H. Q. Fu, X. Q. Huang, H. Chen, Z. J. Lu, I. Baranowski, and Y. J. Zhao, "Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers," *Appl. Phys. Lett.*, vol. 111, no. 15, Oct. 2017, Art. no. 152102, doi: 10.1063/1.4993201.

[8] S. O. Kucheyev, J. S. Williams, and S. J. Pearton, "Ion implantation into GaN," *Mater. Sci. Eng. R Rep.*, vol. 33, nos. 2–3, pp. 51–108, May 2001, doi: 10.1016/S0927-796X(01)00028-6.

[9] Y. Zhang *et al.*, "Vertical GaN junction barrier Schottky rectifiers by selective ion implantation," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1097–1100, Aug. 2017, doi: 10.1109/Led.2017.2720689.

[10] J. K. Sheu and G. C. Chi, "The doping process and dopant characteristics of GaN," *J. Phys. Condensed Matter*, vol. 14, pp. R657–R702, May 2002, doi: 10.1088/0953-8984/14/22/201.

[11] U. Singisetti *et al.*, "Enhancement-mode N-polar GaN MISFETs with self-aligned source/drain regrowth," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 137–139, Feb. 2011, doi: 10.1109/LED.2010.2090125.

[12] J. Guo *et al.*, "MBE-regrown Ohmics in InAlN HEMTs with a regrowth interface resistance of 0.05 Ω·mm," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 525–527, Apr. 2012, doi: 10.1109/LED.2012.2186116.

[13] Y. Yue *et al.*, "InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012, doi: 10.1109/LED.2012.2196751.

[14] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41–43, Jan. 2012, doi: 10.1109/led.2011.2173456.

[15] H. Xing, S. P. DenBaars, and U. K. Mishra, "Characterization of AlGaN/GaNp-n diodes with selectively regrown n-AlGaN by metal-organic chemical-vapor deposition and its application to GaN-based bipolar transistors," *J. Appl. Phys.*, vol. 97, no. 11, 2005, Art. no. 113703, doi: 10.1063/1.1914952.

[16] G. Koblmüller, R. M. Chu, A. Raman, U. K. Mishra, and J. S. Speck, "High-temperature molecular beam epitaxial growth of AlGaN/GaN on GaN templates with reduced interface impurity levels," *J. Appl. Phys.*, vol. 107, no. 4, 2010, Art. no. 043527, doi: 10.1063/1.3285309.

[17] K. Fu *et al.*, "Investigation of GaN-on-GaN vertical $p-n$ diode with regrown p-GaN by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 113, no. 23, Dec. 2018, Art. no. 233502, doi: 10.1063/1.5052479.

[18] I. Stricklin *et al.*, "Investigation of interfacial impurities in m-plane GaN regrown $p-n$ junctions for high-power vertical electronic devices," in *Proc. SPIE*, Sep. 2018, Art. no. 1075402, doi: 10.1117/12.2322005.

[19] M. Azize, Z. Bougrioua, and P. Gibart, "Inhibition of interface pollution in AlGaN/GaN HEMT structures regrown on semi-insulating GaN templates," *J. Cryst. Growth*, vol. 299, no. 1, pp. 103–108, Feb. 2007, [Online]. Available: https://doi.org/10.1016/j.jcrysgro.2006.10.250

[20] W. Lee *et al.*, "Optimization of Fe doping at the regrowth interface of GaN for applications to III-nitride-based heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 90, no. 9, Feb. 2007, Art. no. 93509, doi: 10.1063/1.2535899.

[21] J. P. Liu *et al.*, "III-nitride heterostructure field-effect transistors grown on semi-insulating GaN substrate without regrowth interface charge," *Appl. Phys. Lett.*, vol. 92, no. 13, Mar. 2008, Art. no. 133513, doi: 10.1063/1.2906372.

[22] Z. Hu *et al.*, "1.1-kV vertical GaN $p-n$ diodes with p-GaN regrown by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1071–1074, Aug. 2017, doi: 10.1109/led.2017.2720747.

[23] G. W. Pickrell *et al.*, "Regrown vertical GaN $p-n$ diodes with low reverse leakage current," *J. Electron. Mater.*, vol. 48, no. 5, pp. 3311–3316, May. 2019, doi: 10.1007/s11664-019-07098-6.

[24] T. Yamamoto and H. Katayama-Yoshida, "Materials design for the fabrication of low-resistivity p-type GaN using a codoping method," *Jpn. J. Appl. Phys.*, vol. 36, no. 2, pp. L180–L183, Feb. 1997, doi: 10.1143/jjap.36.l180.

[25] H. Katayama-Yoshida, R. Kato, and T. Yamamoto, "New valence control and spin control method in GaN and AlN by codoping and transition atom doping," *J. Cryst. Growth*, vol. 231, no. 3, pp. 428–436, Oct. 2001, doi: 10.1016/S0022-0248(01)01474-9.

[26] Y. Akatsuka, S. Iwayama, T. Takeuchi, S. Kamiyama, M. Iwaya, and I. Akasaki, "Doping profiles in low resistive GaN tunnel junctions grown by metalorganic vapor phase epitaxy," *Appl. Phys. Exp.*, vol. 12, no. 2, Feb. 2019, Art. no. 025502, doi: 10.7567/1882-0786/aafca8.

[27] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, pp. 170–171.

[28] A. Kumar, S. Arafin, M. C. Amann, and R. Singh, "Temperature dependence of electrical characteristics of Pt/GaN Schottky diode fabricated by UHV e-beam evaporation," *Nanoscale Res. Lett.*, vol. 8, p. 481, Nov. 2013, doi: 10.1186/1556-276X-8-481.

[29] H. Iwano, S. Zaima, and Y. Yasuda, "Hopping conduction and localized states in p-Si wires formed by focused ion beam implantations," *J. Vacuum Sci. Technol. B Microelectron. Nanometer Structures Process. Meas. Phenom.*, vol. 16, pp. 2551–2554, Jul. 1998, doi: 10.1116/1.590208.

[30] D. Yu, C. Wang, B. L. Wehrenberg, and P. Guyot-Sionnest, "Variable range hopping conduction in semiconductor nanocrystal solids," *Phys. Rev. Lett.*, vol. 92, May 2004, Art. no. 216802, doi: 10.1103/PhysRevLett.92.216802.

[31] P. Mark and W. Helfrich, "Space-charge-limited currents in organic crystals," *J. Appl. Phys.*, vol. 33, pp. 205–215, Jan. 1962, doi: 10.1063/1.1728487.
[32] J. A. Röhr, D. Moia, S. A. Haque, T. Kirchartz, and J. Nelson, "Exploring the validity and limitations of the Mott–Gurney law for charge-carrier mobility determination of semiconducting thin-films," *J. Phys. Condens. Matter*, vol. 30, Feb. 2018, Art. no. 105901, doi: 10.1088/1361-648x/aaabad.
[33] M. P. Houng, Y. H. Wang, and W. J. Chang, "Current transport mechanism in trapped oxides: A generalized trap-assisted tunneling model," *J. Appl. Phys.*, vol. 86, no. 3, pp. 1488–1491, Aug. 1999, doi: 10.1063/1.370918.
[34] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, and H. Zhou, "Temperature-dependent forward gate current transport in atomic-layer-deposited Al_2O_3/AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor," *Appl. Phys. Lett.*, vol. 98, no. 16, Apr. 2011, Art. no. 163501, doi: 10.1063/1.3573794.
[35] A. S. Barker and M. Ilegems, "Infrared lattice vibrations and free-electron dispersion in GaN," *Phys. Rev. B, Condens. Matter*, vol. 7, pp. 743–750, Jan. 1973, doi: 10.1103/PhysRevB.7.743.
[36] V. W. L. Chin, T. L. Tansley, and T. Osotchan, "Electron mobilities in gallium, indium, and aluminum nitrides," *J. Appl. Phys.*, vol. 75, no. 11, pp. 7365–7372, Jun. 1994, doi: 10.1063/1.356650.
[37] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, no. 2, Jan. 2006, Art. no. 023703, doi: 10.1063/1.2159547.
[38] C. D. Wang *et al.*, "Deep level defects in n-type GaN grown by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 72, no. 10, pp. 1211–1213, Mar. 1998, doi: 10.1063/1.121016.

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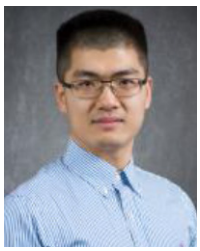

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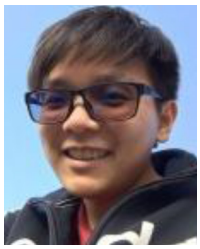

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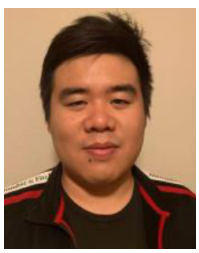

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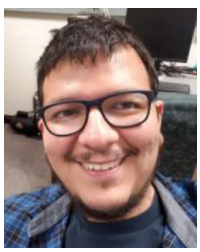

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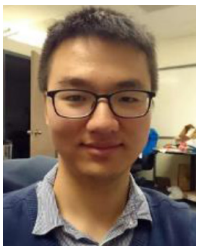

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