High Voltage Vertical GaN p-n Diodes With Hydrogen-Plasma Based Guard Rings

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Abstract—This letter demonstrates novel hydrogenplasma based guard rings (GRs) for high voltage vertical GaN p-n diodes grown on bulk GaN substrates by metalorganic chemical vapor deposition (MOCVD). The GR structure can significantly improve breakdown voltages (*BV*) and critical electric fields (*E_c*) of the devices. Not having field plates or passivation, the p-n diodes with a 9 μ m drift layer and 10 GRs showed *BV*/on-resistance (*R_{on}*) of 1.70 kV/0.65 m Ω ·cm², which are close to the GaN theoretical limit. Moreover, the device also exhibited good rectifying behaviors with an on-current of ~ 2.6 kA/cm², an on/off ratio of ~ 10¹⁰, and a turn-on voltage of 3.56 V. This work represents one of the first effective GR techniques for high performance kV-class GaN p-n diodes.

Index Terms—Gallium nitride, wide bandgap semiconductor, guard ring, p-n diodes, power electronics, edge termination.

I. INTRODUCTION

-NITRIDES have been widely utilized in a variety of photonic and electronic devices [1]–[5]. Due to GaN's wide bandgap, high critical electric field (E_c), and high Baliga's figure of merit (FOM), GaN power electronics has been extensively investigated for efficient power conversion applications [3]–[5]. With the availability of bulk GaN substrates, vertical GaN power devices have been homoepitaxially grown with improved performance compared with lateral devices, such as higher voltage and current handling capability, smaller chip area, better scalability, easier thermal management, and the lack of surface-related issues [3], [6].

Recently, various vertical GaN p-n diodes have been demonstrated on both foreign substrates such as silicon [5], [7]–[10] and bulk substrates [11]–[23]. One of the key targets of

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these efforts is to achieve high breakdown voltages (BV) by alleviating or eliminating the electric field crowding at the junction edge to avoid the premature breakdown [24]. Some reported edge termination techniques in GaN devices include field plates (FPs) and beveled mesas in combination with passivation [18], [19], and partially compensated edge termination [20]–[22]. Guard ring (GR) structures based on selective p-type or highly-resistive (HR) regions are one of the most effective edge termination techniques [25]–[28]. However, there are very few reports on GRs for kV-class GaN p-n power diodes, except a mesa-based GR structure [17].

Ion implantation has usually been used in SiC technology to result in the HR GR structures by creating midgap defect states [25], [26]. Currently, the ion-implantation technique for GaN devices is still under development and face some challenges [29]. Additionally, plasma treatments are also being used to form HR GaN [29]–[32]. For example, it's been reported that hydrogen (H₂) plasma can be utilized to passivate p-GaN into HR GaN [30]-[32]. This is based on the mechanism that Mg and H can form stable chargeneutral Mg-H complexes [33]. The passivated p-GaN has been shown to be very thermally stable as material itself and in devices [30], [32], [33]. In this work, we demonstrate an effective hydrogen-plasma based GR technique for high voltage vertical GaN p-n diodes. The *BV* and E_c of the devices were significantly enhanced.

II. DEVICE FABRICATION

The devices were homoepitaxially grown on n⁺-GaN bulk GaN substrates by metalorganic chemical vapor deposition (MOCVD). The Ga and N sources were trimethylgallium (TMGa) and ammonia (NH₃), respectively. The Si and Mg dopants were incorporated using precursors silane (SiH₄) and bis(cyclopentadienyl)magnesium (Cp2Mg), respectively. The growth temperature was ~ 1050 °C and the carrier gas was H₂. More growth details can be found elsewhere [1]. As shown in Fig. 1(a), 1- μ m-thick n⁺-GaN ([Si] = 2×10¹⁸ cm⁻³) was first grown on the substrates, followed by 9 μ m n⁻-GaN drift layer ([Si] = 2×10^{16} cm⁻³). Then the growth was finished with 500 nm p⁺-GaN ([Mg] = 10^{19} cm⁻³) and 20 nm p⁺⁺-GaN ([Mg] = 10^{20} cm⁻³). The carrier concentration of the drift layer was ~ 10^{16} cm⁻³ according to capacitancevoltage (C-V) measurements [34]. High resolution X-ray diffraction was used to characterize the crystal quality of the device epilayers using the PANalytical X-ray diffractometer system. The full width at half maximum of (002) and (102)



Fig. 1. (a) Schematic view of the cross-section of the epilayers. (b) Fabrication process for the devices with GRs. (c) Cross-sectional schematics of the devices with GRs. (d) Optical microscopy image (top-view) of the p-n diodes with 10 GRs. (e) SEM images of the cross-section of the devices with GRs.

plane rocking curves were 53.2 and 44.9 arcsec, respectively. The dislocation density was estimated to be $\sim 3.4 \times 10^6$ cm⁻² according to the method in [35], indicating the high quality of the homoepitaxial layers.

The fabrication of vertical GaN p-n diodes was carried out using conventional photolithography [(Fig. 1(b)]. It began with ultrasonic sample cleaning in acetone and isopropyl alcohol, followed by the simultaneous formation of anode and GR patterns via photolithography. Before metal depositions by the electron beam evaporation, the samples were treated in oxygen (O₂) plasma to remove any residual photoresists and then briefly dipped in diluted hydrochloric acid (HCl) to remove native surface oxides. The anodes with a diameter of 100 μ m and metal rings for the GRs formation consisted of metal stacks of Pd/Ni/Au annealed by rapid thermal annealing (RTA) at 450 °C in N₂ ambient. The cathodes were non-alloyed metal stacks of Ti/Al/Ni/Au at the backside of the samples.

The metal rings have a nominal width and spacing of 10 μ m and 1.5 μ m, respectively. According to simulations for multiple GRs, the p⁺-GaN ring spacing plays (i.e., the GR width) a critical role: it should be narrow enough especially in the inner circles to enhance the BV, usually 1-2 μ m. The width of p⁺-GaN rings (i.e., the GR spacing) may be further decreased without significantly impacting device performance if the device area needs to be reduced. In addition, a non-uniform GR design can also be implemented where the GR width increases with increasing distance from the main junction. The two types of GR designs are widely used for power devices [24]. More details about the GR geometry design can be found in [24], [36], [37]. It should be noted the metal rings were formed at the same time with the anodes without additional photolithography steps, simplifying the fabrication process.

To form GRs, the samples were loaded into the STS AGE inductively coupled plasma (ICP) tool for H_2 plasma treatments where the metal rings served as hard masks. After thermal annealing by RTA at 400 °C in N₂ ambient, the exposed p-GaN regions were fully passivated by H and become HR GRs. [30] The ICP conditions were as follows: H_2 flow of 25 sccm, ICP power of 300 W, RF power of 5 W, and pressure of 8 mTorr. Figure 1(c) schematically shows the cross-section of the final vertical GaN p-n diodes with



Fig. 2. (a) Current density and ideality factor as a function of anode voltage for the reference sample and GaN p-n diodes with different GRs in a linear scale. (b) Current density and R_{on} versus anode voltage for the reference sample and GaN p-n diodes with different GRs in a semi-log scale.

GRs. Devices with 1, 5 and 10 metal rings were fabricated, which will be referred to as devices with 1, 5 and 10 GRs, respectively, in the following discussions.

Figure 1(d) shows the top-view image of the p-n diodes with 10 GRs by optical microscope. Scanning electron microscope (SEM) images in Fig. 1(e) clearly identified the p⁺-GaN regions and the GR regions. They had very different secondary electron (SE) contrasts. The SE emission from GR regions showed the similar contrast to that of n⁻-GaN, suggesting the deactivation of Mg acceptors. More details about the mechanisms and the interpretation of SE contrasts can be found in [38]. The p-n diodes without metal rings were also fabricated for reference. No FPs or passivation were employed in this work. Forward current–voltage (*I*–*V*) curves were measured by Keithley 2400 sourcemeter. Breakdown measurements were conducted using Tektronix 370A curve tracer where the samples were immersed in Fluorinert FC-70 to avoid flash-over.

III. EXPERIMENTAL RESULTS

Figure 2(a) presents the forward I-V characteristics and ideality factors (*n*) of the reference p-n diodes and p-n diodes with 1 GR, 5 GRs and 10 GRs in a linear scale. By linear extrapolation, the turn-on voltages (V_{on}) for the four samples were extracted as 3.50, 3.53, 3.59, and 3.56 V, respectively. The minimum *n* were 1.69, 1.65, 1.67, and 1.64 for the four samples, respectively. The *n* first decreased and then increased. The former was caused by the transition from the Shockley-Read-Hall (SRH) recombination current to the p-n diode diffusion current, and the latter was due to the series resistance [18].

Figure 2(b) shows forward I-V characteristics and the specific on-resistance (R_{on}) for the four samples in a semi-log scale. They had an on-current of ~ 2.6 kA/cm² and an on/off ratio of ~ 10¹⁰. The R_{on} of the four samples were 0. 65, 0.63, 0.70, and 0.65 m Ω ·cm², respectively. Furthermore, strong light emission was observed from all samples at high forward biases due to the radiative recombination in the p-n diode depletion region, which usually indicates the high material quality of the devices [39]. Electroluminescence analysis revealed there were 3.4 eV, 3.2 eV and 2.2 eV emission peaks, which are due to band-edge emission, donor-acceptor-pair transition, and deeplevel transition, respectively. These results show the p-n diodes with GRs have similar forward characteristics to the reference sample, which is desired and also good for the fair breakdown comparisons among these samples.

Figure 3(a) shows the breakdown measurements for the reference sample and the samples with 1 GR, 5 GRs and 10 GRs.



Fig. 3. (a) Reverse breakdown measurements for the reference sample and samples with different GRs by Tektronix 370A curve tracer. (b) The critical electric field for the four samples. (c) The calculated electric field profiles of the four samples along the vertical direction of the p-n diodes.

 TABLE I

 Device Parameters for the Four GaN p-n Diodes

	п	V _{on} (V)	R_{on} (m $\Omega \cdot \mathrm{cm}^2$)	<i>BV</i> (kV)	E_c (MV/cm)
Reference	1.69	3.50	0.65	1.08	2.11
1 GR	1.65	3.53	0.63	1.39	2.50
5 GRs	1.67	3.59	0.70	1.58	2.67
10 GRs	1.64	3.56	0.65	1.70	2.80

The breakdown of the devices was edge breakdown with catastrophic damages at the device edge, as confirmed using the optical microscope. The BV of the four samples were 1.08, 1.39, 1.58, and 1.70 kV, respectively. The breakdown capability of the GaN p-n diodes was significantly enhanced by the addition of GRs. And the BV was increased with the increasing number of GRs. This is because more GRs can better spread the electric field laterally at the device edge, which is consistent with previous reports [24], [40]. Furthermore, the reverse breakdown and leakage characteristics of the devices at elevated temperatures and reliability are undergoing topics [30].

In punch-through structures, E_c is related to BV using the following equation [18]

$$BV = E_c d - \frac{e N_D d^2}{2\varepsilon_0 \varepsilon_r} \tag{1}$$

where e is the electron charge, d and N_D are the thickness and carrier concentration of the drift layer, ε_0 is the permittivity of the vacuum, and ε_r is the relative permittivity of GaN. The calculated E_c of the four samples were 2.11, 2.50, 2.67, and 2.80 MV/cm, respectively, as shown in Fig. 3(b). E_c was increased dramatically with the increasing number of GRs, sharing a similar trend to the BV. As a comparison to previous reports, if assuming that 75% of the entitled BV is achieved as in [14], [18], the p-n diodes with 10 GRs exhibited the highest E_c of 3.43 MV/cm, which is among the best values ever reported for GaN p-n diodes [6], [14], [15], [18], [39]. With the one-dimensional Poisson's equation, the electric field profiles of the samples were also calculated in Fig. 3(c). Table I summarizes the device parameters for the four GaN p-n diodes. These results indicate employing the hydrogen-plasma based GRs is very effective in enhancing the breakdown capability and E_c of GaN p-n diodes without degrading their forward characteristics.

Figure 4 shows the benchmark plot of R_{on} vs. BV for vertical GaN p-n diodes on silicon and bulk GaN



Fig. 4. R_{on} versus BV of vertical GaN p-n diodes on silicon and GaN substrates [7]–[20]. As-reported values are used for all the references expect that R_{on} in Ref. [18] and [19] were recalculated using the anode for a direct comparison based on [41] and [42]. The circled region shows the devices in this work.

substrates [7]–[20]. The performance of our devices with GRs is close to the theoretical limit line of GaN. It should be noted that our devices only had a drift layer thickness of 9 μ m without FPs or passivation. The 1.70 kV/0.65 m $\Omega \cdot \text{cm}^2$ of our GaN p-n diodes with 10 GRs is comparable to performance of demonstrated best devices with similar and/or thicker drift layer thicknesses [14]–[19]. These results have demonstrated that with the simple hydrogen-plasma based GR structure, the performance of kV-class GaN p-n diodes can be significantly improved.

IV. CONCLUSION

We have demonstrated a novel hydrogen-plasma based GR technique for vertical GaN p-n diodes. The *BV* and E_c were dramatically enhanced by the GRs. In addition, the devices also exhibited good forward characteristics with a R_{on} of 0.65 m Ω ·cm² and an on/off ratio of ~ 10¹⁰. With a 9 μ m drift layer and the simple GR technique, 1.70 kV/0.65 m Ω ·cm² was achieved, which is close to the theoretical limit. These results indicate the hydrogen-plasma based GRs are very effective for high performance kV-class GaN p-n diodes.

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REFERENCES

- Y. Zhao, H. Fu, G. T. Wang, and S. Nakamura, "Toward ultimate efficiency: Progress and prospects on planar and 3D nanostructured nonpolar and semipolar InGaN light-emitting diodes," *Adv. Opt. Photon.*, vol. 10, no. 1, pp. 246–308, Feb. 2018, doi: 10.1364/AOP.10.000246.
- [2] H. Fu, Z. Lu, X. Huang, H. Chen, and Y. Zhao, "Crystal orientation dependent intersubband transition in semipolar AlGaN/GaN single quantum well for optoelectronic applications," *J. Appl. Phys.*, vol. 119, no. 17, May 2016, Art. no. 174502, doi: 10.1063/1.4948667.
- [3] S. Chowdhury and U. K. Mishra, "Lateral and vertical transistors using the AlGaN/GaN heterostructure," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3060–3066, Oct. 2013, doi: 10.1109/TED.2013.2277893.
- [4] D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Large-area *in-situ* oxide, GaN interlayer-based vertical trench MOSFET (OG-FET)," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 711–714, May 2018, doi: 10.1109/LED.2018.2813312.
- [5] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: A review and outlook," *J. Phys. D, Appl. Phys.*, vol. 51, no. 27, May 2018, Art. no. 273001, doi: 10.1088/1361-6463/aac8aa.

- [6] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical power p-n diodes based on bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015, doi: 10.1109/TED.2014.2360861.
- [7] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-m Ω·cm² fully vertical GaN-on-Si power diodes by selective removal of Si substrates and buffer layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.
- [8] S. Mase, T. Hamada, J. J. Freedsman, and T. Egawa, "Effect of drift layer on the breakdown voltage of fully-vertical GaN-on-Si p-n diodes," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1720–1723, Dec. 2017, doi: 10.1109/LED.2017.2765340.
- [9] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully vertical GaN p-i-n diodes using GaN-on-Si epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/ LED.2016.2548488.
- [10] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si quasi-vertical p-i-n diodes with BFOM of 2.0 GW/cm²," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.
- [11] Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, "High-breakdown-voltage pn-junction diodes on GaN substrates," *J. Cryst. Growth*, vol. 298, pp. 875–878, Jan. 2007, doi: 10.1016/j.jcrysgro.2006.10.246.
- [12] T.-T. Kao, J. Kim, T.-C. Lee, M.-H. Ji, T. Detchprohm, R. D. Dupuis, and S.-C. Shen, "Homojunction GaN p-i-n rectifiers with ultralow onstate resistance," in *Proc. CSMANTECH Conf.*, May 2014, pp. 157–160.
- [13] H. Fu, X. Huang, H. Chen, Z. Lu, X. Zhang, and Y. Zhao, "Effect of buffer layer design on vertical GaN-on-GaN p-n and Schottky power diodes," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 763–766, Jun. 2017, doi: 10.1109/LED.2017.2690974.
- [14] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, "High voltage vertical GaN p-n diodes with avalanche capability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3067–3070, Oct. 2013, doi: 10.1109/TED.2013.2266664.
- [15] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 247–249, Feb. 2014, doi: 10.1109/LED.2013.2294175.
- [16] Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, "High-breakdown-voltage and lowspecific-on-resistance GaN p-n junction diodes on free-standing GaN substrates fabricated through low-damage field-plate process," *Jpn. J. Appl. Phys.*, vol. 52, Jan. 2013, Art. no. 028007, doi: 10.7567/JJAP.52.028007.
- [17] H. Ohta, K. Hayashi, F. Horikiri, M. Yoshino, T. Nakamura, and T. Mishima, "5.0 kV breakdown-voltage vertical GaN p–n junction diodes," *Jpn. J. Appl. Phys.*, vol. 57, no. 4S, Feb. 2018, Art. no. 04FG09, doi: 10.7567/JJAP.57.04FG09.
- [18] K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "1.7-kV and 0.55-mΩ·cm² GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.
- [19] K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ·cm²: A record high figure-of-merit of 12.8 GW/cm²," in *IEDM Tech. Dig.*, Dec. 2015, pp. 971–974, doi: 10.1109/IEDM.2015.7409665.
- [20] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, "High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination," *Appl. Phys. Lett.*, vol. 113, no. 2, Jul. 2018, Art. no. 023502, doi: 10.1063/1.5035267.
- [21] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, "High voltage vertical p-n diodes with ion-implanted edge termination and sputtered SiNx passivation on GaN substrates," in *IEDM Tech. Dig.*, Dec. 2017, pp. 9.6.1–9.6.4, doi: 10.1109/IEDM.2017.8268361.
- [22] J. Wang, R. McCarthy, C. Youtsey, R. Reddy, J. Xie, E. Beam, L. Guido, L. Cao, and P. Fay, "High-voltage vertical GaN p-n diodes by epitaxial liftoff from bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1716–1719, Nov. 2018, doi: 10.1109/LED.2018.2868560.
- [23] H. Fu, K. Fu, X. Huang, H. Chen, I. Baranowski, T.-H. Yang, J. Montes, and Y. Zhao, "High performance vertical GaN-on-GaN pn power diodes with hydrogen-plasma-based edge termination," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1018–1021, Jul. 2018, doi: 10.1109/LED.2018.2837625.

- [24] B. J. Baliga, Fundamentals of Power Semiconductor Devices. New York, NY, USA: Springer-Verlag, 2008, ch. 3, pp. 91–155.
- [25] B. J. Baliga, Silicon Carbide Power Devices. Singapore: World Scientific, 2005, ch. 3, pp. 37–70.
- [26] D. Alok and B. J. Baliga, "SiC device edge termination using finite area argon implantation," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 1013–1017, Jun. 1997, doi: 10.1109/16.585559.
- [27] C.-H. Lin, Y. Yuda, M. H. Wong, M. Sato, N. Takekawa, K. Konishi, T. Watahiki, M. Yamamuka, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Vertical Ga₂O₃ Schottky barrier diodes with guard ring formed by nitrogen-ion implantation," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1487–1490, Sep. 2019, doi: 10.1109/LED.2019.2927790.
- [28] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, ch. 3, pp. 181–184.
- [29] S. Han, S. Yang, and K. Sheng, "High-voltage and high-I_{ON}/I_{OFF} vertical GaN-on-GaN Schottky barrier diode with nitridation-based termination," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 572–575, Apr. 2018, doi: 10.1109/LED.2018.2808684.
- [30] H. Fu, K. Fu, H. Liu, S. R. Alugubelli, X. Huang, H. Chen, J. Montes, T.-H. Yang, C. Yang, J. Zhou, F. A. Ponce, and Y. Zhao, "Implantationand etching-free high voltage vertical GaN p-n diodes terminated by plasma-hydrogenated p-GaN: Revealing the role of thermal annealing," *Appl. Phys. Exp.*, vol. 12, no. 5, May 2019, Art. no. 051015, doi: 10.7567/1882-0786/ab1813.
- [31] R. Hao, K. Fu, G. Yu, W. Li, J. Yuan, L. Song, Z. Zhang, S. Sun, X. Li, Y. Cai, X. Zhang, and B. Zhang, "Normally-off p-GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment," *Appl. Phys. Lett.*, vol. 109, Oct. 2016, Art. no. 152106, doi: 10.1063/1.4964518.
- [32] R. Hao, N. Xu, G. Yu, L. Song, F. Chen, J. Zhao, X. Deng, X. Li, K. Cheng, K. Fu, Y. Cai, X. Zhang, and B. Zhang, "Studies on fabrication and reliability of GaN high-resistivity-cap-layer HEMT," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1314–1320, Apr. 2018, doi: 10.1109/TED.2018.2803521.
- [33] S. Nakamura, N. Iwasa, M. Senoh, and T. Mukai, "Hole compensation mechanism of P-type GaN films," *Jpn. J. Appl. Phys.*, vol. 31, no. 5A, pp. 1258–1266, May 1992, doi: 10.1143/JJAP.31.1258.
- [34] H. Fu, I. Baranowski, X. Huang, H. Chen, Z. Lu, J. Montes, X. Zhang, and Y. Zhao, "Demonstration of AlN Schottky barrier diodes with blocking voltage over 1 kV," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1286–1289, Sep. 2017, doi: 10.1109/LED.2017.2723603.
- [35] H. Fu, X. Huang, H. Chen, Z. Lu, I. Baranowski, and Y. Zhao, "Ultralow turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers," *Appl. Phys. Lett.*, vol. 111, no. 15, Oct. 2017, Art. no. 152102, doi: 10.1063/1.4993201.
- [36] D. C. Sheridan, G. F. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, and C.-C. Tin, "Design and fabrication of planar guard ring termination for high-voltage SiC diodes," *Solid-State Electron.*, vol. 44, no. 8, pp. 1367–1372, Aug. 2000, doi: 10.1016/S0038-1101(00)00081-2.
- [37] J. R. Laroche, F. Ren, K. W. Baik, S. J. Pearton, B. S. Shelton, and B. Peres, "Design of edge termination for GaN power Schottky diodes," *J. Electrochem. Mater.*, vol. 34, no. 4, pp. 370–374, Apr. 2005, doi: 10.1007/s11664-005-0113-6.
- [38] S. R. Alugubelli, H. Fu, K. Fu, H. Liu, Y. Zhao, and F. A. Ponce, "Dopant profiling in p-i-n GaN structures using secondary electrons," *J. Appl. Phys.*, vol. 126, no. 1, Jul. 2019, Art. no. 015704, doi: 10.1063/1.5096273.
- [39] M. Qi, K. Nomoto, M. Zhu, Z. Hu, Y. Zhao, V. Protasenko, B. Song, X. Yan, G. Li, J. Verma, S. Bader, P. Fay, H. G. Xing, and D. Jena, "High breakdown single-crystal GaN p-n diodes by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 107, Dec. 2015, Art. no. 232101, doi: 10.1063/1.4936891.
- [40] W. Sung, E. van Brunt, B. J. Baliga, and A. Q. Huang, "A new edge termination technique for high-voltage devices in 4H-SiCmultiple-floating-zone junction termination extension," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 880–882, Jul. 2011, doi: 10.1109/LED.2011.2144561.
- [41] Z. Hu, K. Nomoto, M. Qi, W. Li, M. Zhu, X. Gao, D. Jena, and H. G. Xing, "1.1-kV vertical GaN p-n diodes with p-GaN regrown by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1071–1074, Aug. 2017, doi: 10.1109/LED.2017.2720747.
- [42] K. Fu, H. Fu, X. Huang, H. Chen, T.-H. Yang, J. Montes, C. Yang, J. Zhou, and Y. Zhao, "Demonstration of 1.27 kV etch-then-regrow GaN p–n junctions with low leakage for GaN power electronics," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1728–1731, Nov. 2019, doi: 10.1109/LED.2019.2941830.