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Normally-off AlN/β-Ga_2O_3 field-effect transistors using polarization-induced doping

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Abstract

III-nitrides and beta-phase gallium oxide (β-Ga_2O_3) are currently two intensively investigated wide bandgap semiconductor materials for power electronics. Due to the relatively low lattice mismatch between the two material systems and the availability of bulk AlN, GaN and β-Ga_2O_3 substrates, epitaxial growth of III-nitrides on β-Ga_2O_3 or vice versa has been realized. However, the design of power devices by integrating the two material systems is still lacking. Here we numerically investigate an AlN/β-Ga_2O_3 heterostructure by taking advantage of polarization-induced doping to realize high-performance enhancement-mode transistors. Induced by polarization effects at the AlN/β-Ga_2O_3 interface, a 2-dimensional electron gas concentration can reach up to 8.1×10^{19} cm^{-3} in the channel. On top of the channel, a p-GaN gate was introduced and eventually a normally-off AlN/β-Ga_2O_3 field-effect transistor with tunable positive threshold voltages was realized. Furthermore, we inserted an unintentionally doped GaN back barrier layer to suppress the drain leakage current. Eventually, the transfer and output characteristics of the proposed device with different structural parameters were further investigated and analyzed in the pursuit of high-performance III-nitrides/Ga_2O_3-based power devices.

Keywords: β-Ga_2O_3, p-GaN gate, field-effect transistors, normally-off, polarization-induced doping

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, beta-phase gallium oxide (β-Ga_2O_3) has attracted considerable attention due to its unique material properties such as wide bandgap (4.7 eV), high breakdown field (8 MV cm^{-1}) and high saturation velocity ($\sim 2 \times 10^7$ cm s^{-1}) for photodetector and power device applications [1–6]. Various β-Ga_2O_3 power electronic devices have been demonstrated, including Schottky barrier diodes (SBDs) [7–9] and field effect transistors (FETs) [10, 11].

Owing to the nonpolar nature of β-Ga_2O_3 crystals, modulation-doped heterostructure is one of the possible approaches to realize Ga_2O_3-based FETs. Recently, a modulation-doped two-dimensional electron gas (2DEG) at the β-$(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$ heterojunction by silicon delta doping (δ-doping) has been reported [12], followed by the demonstration of modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ double heterostructure FETs [13]. However, the control of δ-doping, such as the position and concentration of the δ-doping, is rather challenging through the epitaxial growth

process. Fortunately, due to the presence of large spontaneous and piezoelectric polarization charges at nitride-based heterostructures (for example, the AlGaN/GaN heterostructure), an effective δ-doping can be created at the sharp heterointerface with atomic control and carrier concentration far beyond what is achievable by the impurity-based δ-doping technology [14]. Therefore, to further improve the performance of β-Ga_2O_3 based FETs, considering the advantage of the high breakdown field of Ga_2O_3 material and strong polarization fields of III-nitrides, a combination of the nonpolar β-Ga_2O_3 with polar III-nitrides to form a III-nitride/β-Ga_2O_3 heterostructure could be a promising device architecture to realize high-performance power electronics [15–18].

Moreover, due to the presence of 2DEG in the channel at zero gate bias, the β-$(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$ modulation-doped FET showed a normally-on operation [12]. However, normally-off enhancement mode devices with positive threshold voltages (V_{th}) are highly desirable in power electronics applications, especially in designing fail-safe power switches, RF power amplifiers, and simplified driving circuits [19, 20]. To pursue the normally-off devices, there are several device structures being proposed: metal-insulator-semiconductor FET (MISFET) [21, 22], fluorine implantation under the gate [23, 24], p-GaN gate [25–27] and Cascode configuration [28]. Among those structures, it is generally accepted that the p-GaN-based gate is a relatively stable and reliable approach. The V_{th} is not affected by the interface states at the channel as in the MISFETs, and it is stable over time as opposed to the devices based on fluorine implantation [29, 30].

In this work, we propose a p-GaN gated FET structure based on Al-polar AlN/β-Ga_2O_3 heterojunction. The proposed device structure can be possibly realized via those mature growth techniques such as MOCVD, MBE, or PLD since many studies have been carried out in the investigation of the growth process of nitrides/Ga_2O_3 heterostructures in the past [15, 31–34]. The band diagram and 2DEG concentration at the interface of the heterostructure were investigated. It was found that a channel is formed at the interface with a high 2DEG concentration due to the band offset and polarization effects. A p-GaN gate was employed to obtain a normally-off operation with a positive V_{th}. In order to suppress the drain leakage current, a Ga-polar UID GaN back barrier layer was inserted so that positive polarization charges can be formed at the interface. Those positive charges can draw the electrons away from the bulk Ga_2O_3 (the region below the channel) and thus form a high-resistive region to suppress the leakage current. Herein, we demonstrated a polarization-induced-doped field effect transistor (PIDFET), where its electrical characteristics were comprehensively investigated and computed by a 2D device drift-diffusion-based simulation (Silvaco Atlas).

2. Simulation

2.1. Device structures

Simulations for the normally-off III-nitride/β-Ga_2O_3 PIDFET were carried out using a 2D device simulator Silvaco Atlas. As shown in figure 1, the designed PIDFET consisted of a 70 nm p-type doped GaN cap layer with varying gate length (0.1, 0.2, 0.3, 0.4 μm) and hole concentration (1×10^{17}, 1×10^{18}, 2×10^{18}, 4×10^{18}, 6×10^{18} cm^{-3}), a UID Al-polar AlN polarization layer with different thickness (from 4 to 14 nm), 100 nm of UID β-Ga_2O_3 channel layer, and a 100 nm of UID Ga-polar GaN back barrier layer. For comparison, we also designed a structure without this GaN back barrier layer to show its effect on the leakage current suppression. Two 20 nm thick heavily n-doped β-Ga_2O_3 contact layers were adopted under the source/drain to reduce the serial resistance and enhance the device working current. The source-drain and the gate-source spacing were set as 1.3 μm and 0.2 μm, respectively. Aluminum (work function: 4.6 eV) was used for the gate Schottky contact. As for the source and drain, the ideal ohmic contacts were implemented in carrying out the simulation. It is suggested to have ohmic contacts to measure the device performance in device fabrication and demonstration. In the real device implementation, we need to carefully control the surface donor since it significantly impacts the device performance [35, 36], thus, in our simulation setup, we included a thick layer of silicon oxide to passivate the AlN layer. We normally use silicon oxide or silicon nitride as the passivation layer [37].

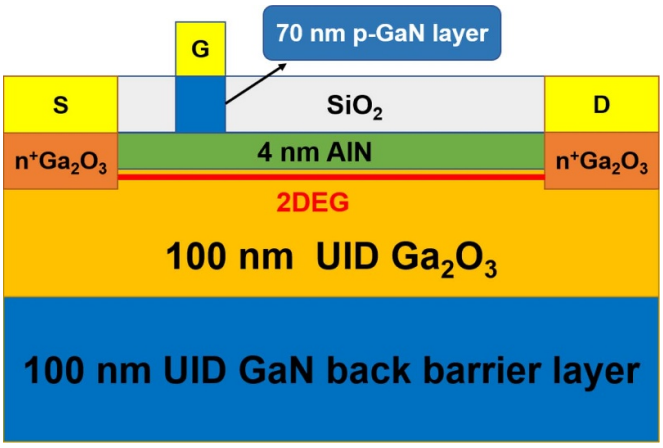

Figure 1. Schematic structure of p-GaN gated PIDFET composed of AlN/β-Ga_2O_3/GaN.

2.2. Physical models

The material structure, spontaneous polarization (P_{SP}), and piezoelectric polarization (P_{PZ}) parameters were calibrated in the simulation to produce correct polarization charges at the heterointerface according to the following equations [38]

$$P_{tot} = P_{sp} + P_{pz} \tag{1}$$

$$P_{pz} = e_{33}\varepsilon_{zz} + e_{31}\left(\varepsilon_{xx} + \varepsilon_{yy}\right) \tag{2}$$

$$\varepsilon_{zz} = \left(c - c_0\right)/c_0,\ \varepsilon_{xx} = \varepsilon_{yy} = \left(a - a_0\right)/a_0 \tag{3}$$

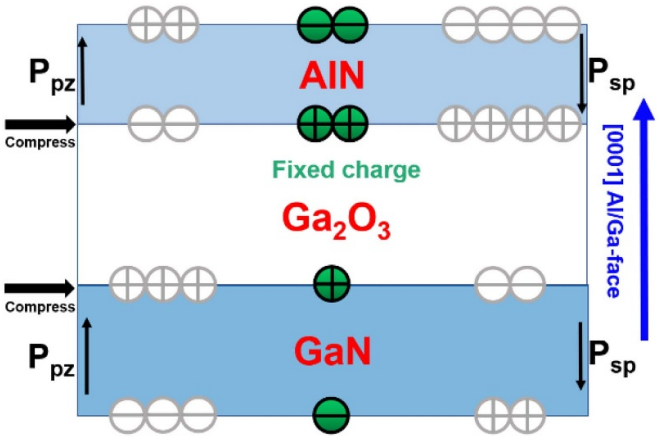

Figure 2. Polarization charge distribution schematic of PIDFET (AlN/β-Ga_2O_3/GaN).

Table 1. Parameters used for polarization calculation of AlN/β-Ga_2O_3/GaN heterostructure.

	Lattice mismatch with β-Ga_2O_3	e_{33} (C m^{-2})	e_{31} (C m^{-2})	P_{sp} (C m^{-2})
AlN	2.4% [15]	1.46 [38]	−0.60 [38]	−0.081 [38]
GaN	4.7% [32]	0.73 [38]	−0.49 [38]	−0.029 [38]

where P_{tot} is the total polarization, P_{sp} and P_{pz} are the spontaneous polarization and piezoelectric polarization, respectively, e_{33} and e_{31} are piezoelectric coefficients parallel and perpendicular to the c axis, respectively, ε_{xx} and ε_{yy} are the biaxial stresses in c plane, and ε_{zz} is the stress along the c axis.

Table 1 lists polarization related parameters that used for AlN/β-Ga_2O_3/GaN heterostructure. It is worth noting that the proposed III-nitride/β-Ga_2O_3 heterojunctions are all based on the (−201) plane of β-Ga_2O_3 and (001) of III-nitride. A very small lattice mismatch (∼2.4%) between the AlN and β-Ga_2O_3 was adopted [15]. At the interface between Al-polar AlN and βGa_2O_3, P_{SP} is dominant and induces an electric field along the growth direction and thus provides a driving force for the electron flowing into the channel. At the β-Ga_2O_3/Ga-polar GaN interface, P_{PZ} dominates polarization charges and a reverse electric direction is formed, drawing the electrons from bulk Ga_2O_3 (the region beneath the 2DEG channel). The interface charge distributions of those two interfaces are schematically shown in figure 2.

The calculated energy band diagram (red line) and electron distribution (blue line) at the AlN/β-Ga_2O_3 and the β-Ga_2O_3/GaN heterointerface are shown in figure 3(a). According to the diagram, there are obvious conduction band offsets at both interfaces and high concentration of 2DEGs can be formed. The electron concentration as high as 8.1×10^{19} cm^{-3} was obtained at the upper interface, providing a conductive channel for the PIDFET. The electron density of the bulk Ga_2O_3 was controlled down to 1.36×10^{16} cm^{-3} due to the existence of the GaN back barrier layer which can be further confirmed in figures 3(b) and (c). This much reduced electron

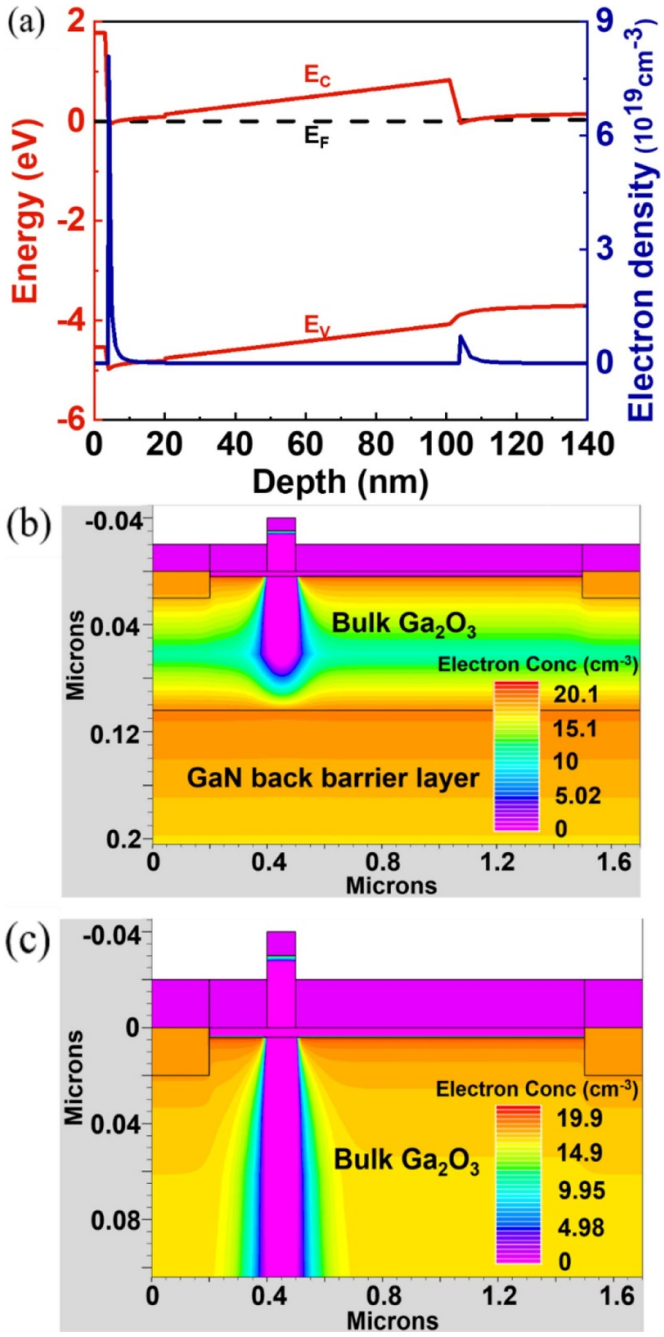

Figure 3. P-GaN gated PIDFET (AlN/β-Ga_2O_3/GaN): (a) energy band diagram and electron density distribution; electron concentration of different layers of (b) device with GaN back barrier layer and of (c) device without GaN back barrier layer. Note: the gate bias (V_{gs}) and drain bias (V_{ds}) for the simulation (b) and (c) are both 0.

density can suppress the drain leakage current and decrease the subthreshold swing.

The models used in the simulations include parallel electric field model for velocity saturation (FLDMOB), Shockley–Read–Hall model (SRH), Fermi–Dirac model (FERMI), incomplete ionization model (INCOMPLETE) and polarization model (POLARIZATION). The Caughey–Thomas expression for β-Ga_2O_3 was also applied with a saturation velocity of 2×10^7 cm s^{-1} and a channel hall mobility

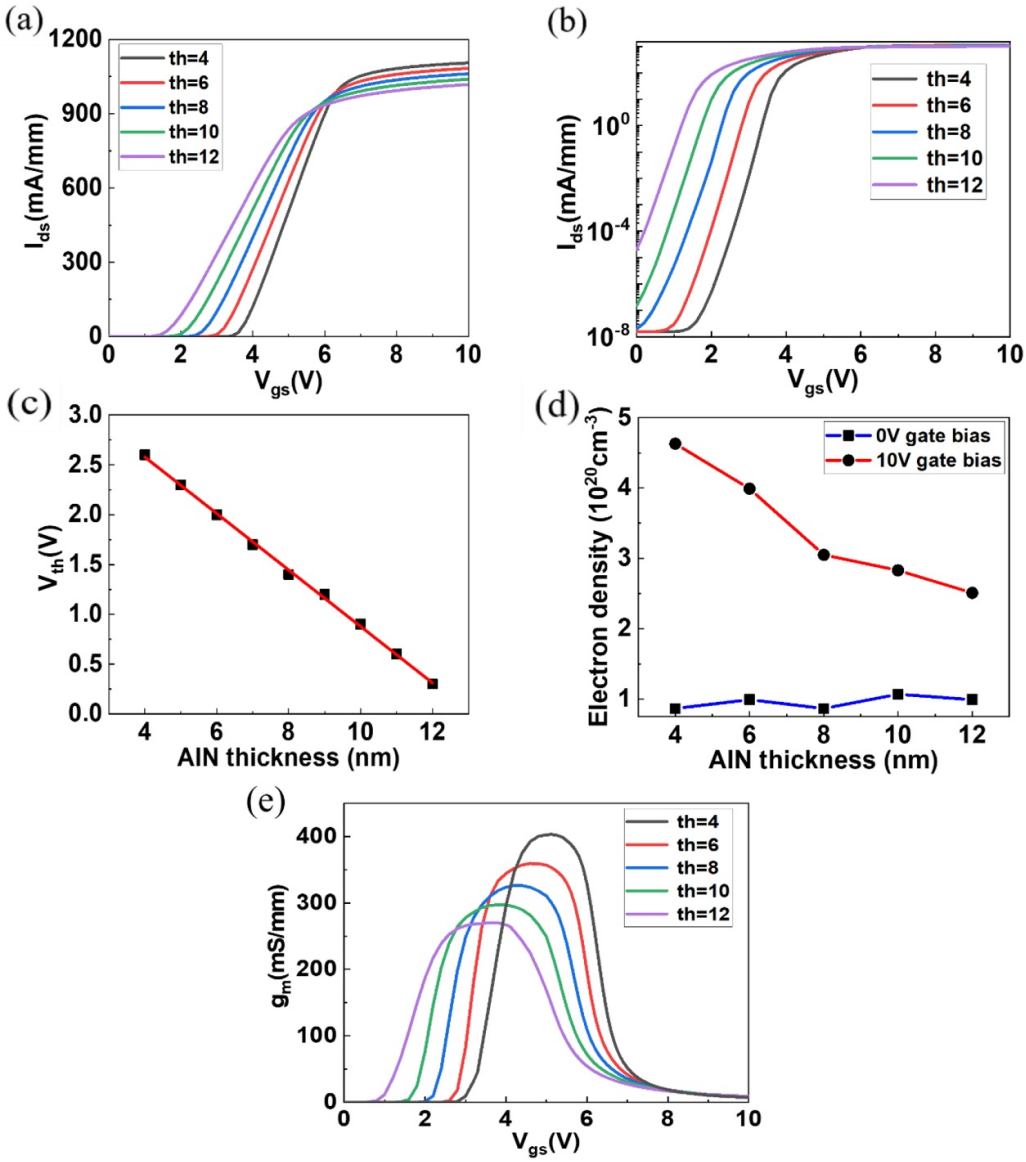

Figure 4. Simulated transfer characteristics with varying AlN thickness of 4, 6, 8, 10 and 12 nm in (a) linear and (b) semi-logarithmic scale; (c) linearly dependent V_{th} vs AlN thickness curve extracted from (b); (d) electron density in the channel with varying AlN thickness at 10 V and 0 V gate biases, respectively; and (e) g_m–V_{gs} curves with varying AlN thickness of 4, 6, 8, 10 and 12 nm.

of 200 cm^2 V^{-1} s^{-1}. These two are typical values for β-Ga_2O_3 based field-effect transistors [39]. We have validated our polarization model by performing calculation on the 2DEG in the AlN/GaN [40] and AlGaN/GaN heterostructures [41, 42], and similar results were obtained. Additionally, it has to be noted that those polarization parameters can be significant different in the calculation of polarization field in those heterostructures if different reference models are adopted (zincblende or hexagonal references) [43]. Moreover, the electron transport model was also calibrated by doing the simulation on an $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFET experimentally reported before [12]. In addition, the channel mobility in this AlN/β-Ga_2O_3 PIDFET may be higher than that in $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFET due to the elimination of the alloy scattering which is one of the significant scattering mechanisms for the electron transportation [43]. The p-type doped buffer was simulated with incomplete ionization model due to the nature of the dopant material (usually Mg in the case of III-nitrides) [44]. All UID layers in the simulator were doped with a low donor background concentration of 10^{15} cm^{-3}. In the following section, the influences of some key structural and device parameters on the device performance are investigated in detail, including AlN polarization layer, p-GaN gate layer and GaN back barrier layer.

3. Results and discussions

3.1. AlN polarization layer

Figures 4(a) and (b) show the simulated transfer characteristics with varying AlN thickness in linear and semi-logarithmic scale, respectively. The V_{th} and the saturation current

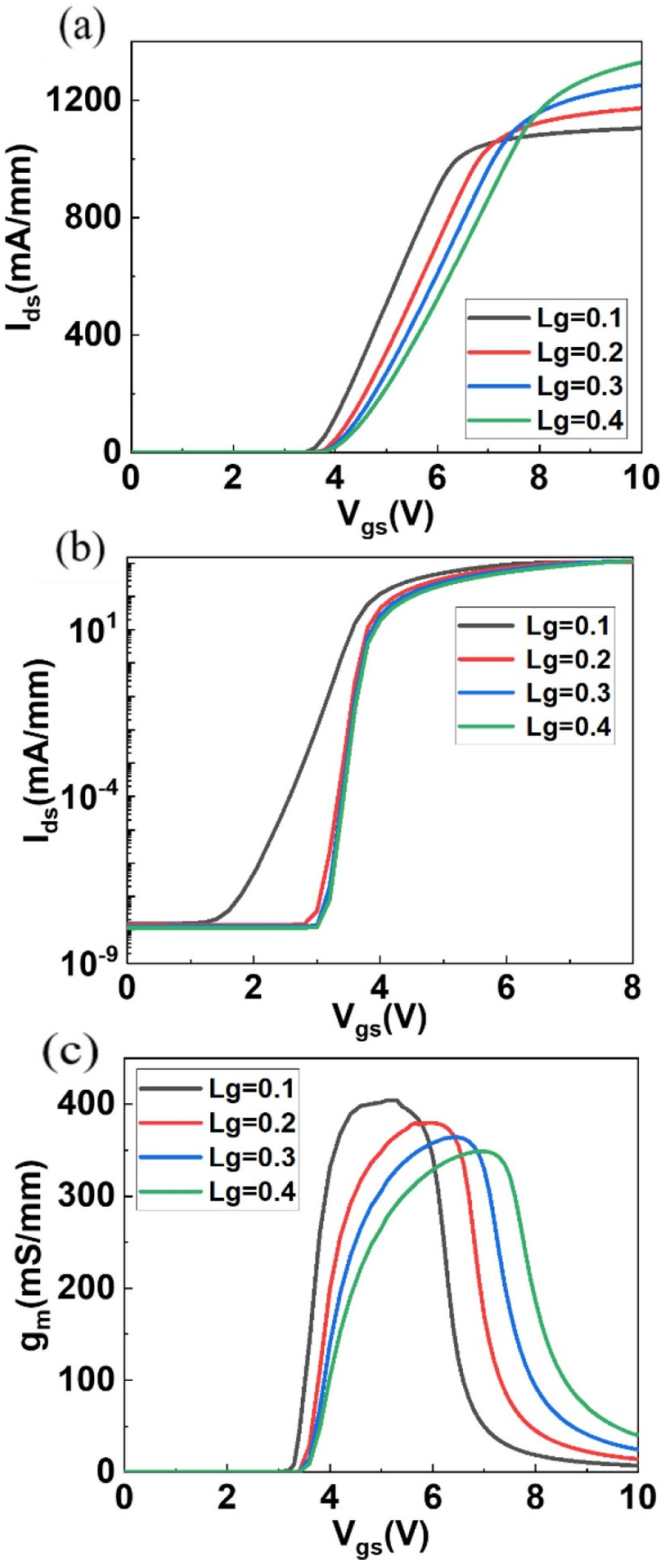

Figure 5. I_{ds}–V_{gs} curves with varying gate length of 0.1, 0.2, 0.3 and 0.4 μm in (a) linear and (b) semi-logarithmic scale, respectively; (c) g_m–V_{gs} curves with varying gate length of 0.1, 0.2, 0.3 and 0.4 μm.

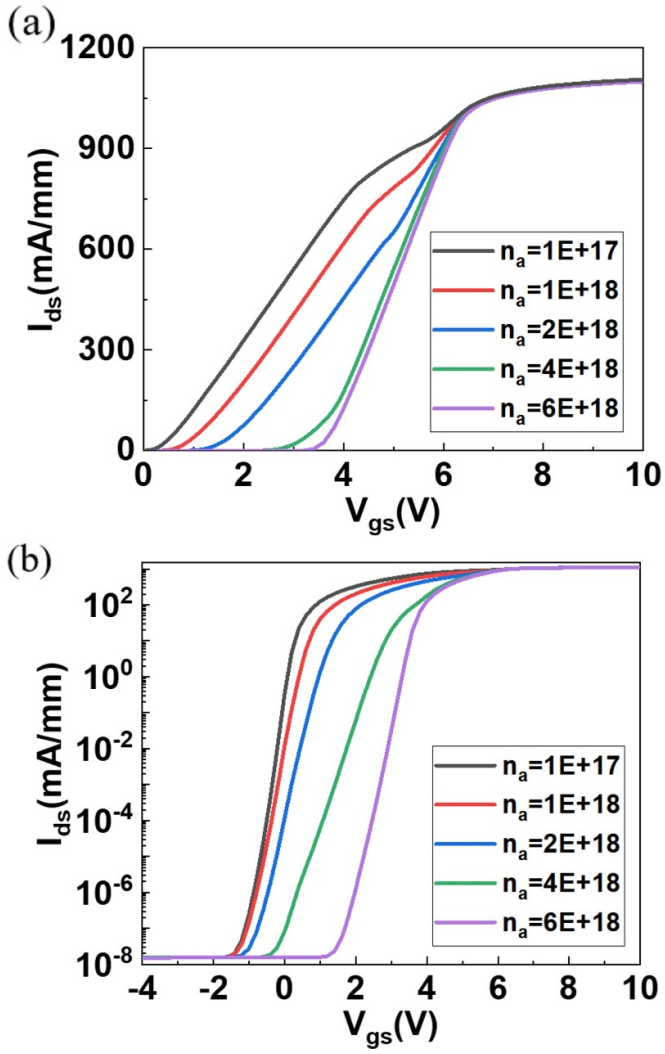

Figure 6. Simulated transfer characteristic with different p-GaN gate acceptor concentration of 1×10^{17}, 1×10^{18}, 2×10^{18}, 4×10^{18} and 6×10^{18} cm^{-3} in (a) linear and (b) semi-logarithmic scale, respectively.

increased with decreasing AlN thickness. The V_{th} values extracted from the semi-logarithmic I_{ds}-V_{gs} curves are 0.3, 0.9, 1.4, 2.0 and 2.6 V for AlN thicknesses of 12, 10, 8, 6 and 4 nm, respectively, as shown in figure 4(b). Further analysis reveals that V_{th} is linearly dependent on the AlN thickness, as plotted in figure 4(c). This means the V_{th} is tunable by varying AlN thickness, and it provides a straightforward approach to achieving the desired V_{th}.

Another obvious trend can be found in figure 4(a) is that the saturation current increases with a decreasing AlN thickness. It is well known that the current density is formulated as equation: $J = -nq\overline{v_d} = nq\mu E$, where n is the electron density, q is the charge of an electron, $\overline{v_d}$ is the average electron drift velocity, μ is the electron mobility, and E is the lateral electric field intensity. The increment of the saturation current can be explained by an enhanced electron density in the channel with a thinner AlN thickness, as shown in figure 4(d). At the gate bias of 0 V, the electron density in the channel, which is only influenced by the polarization charges at the interface, remains almost a constant with varying AlN thickness. At the gate bias of 10 V, however, the electric potential in the channel gets higher and assists the polarization electric field in forming

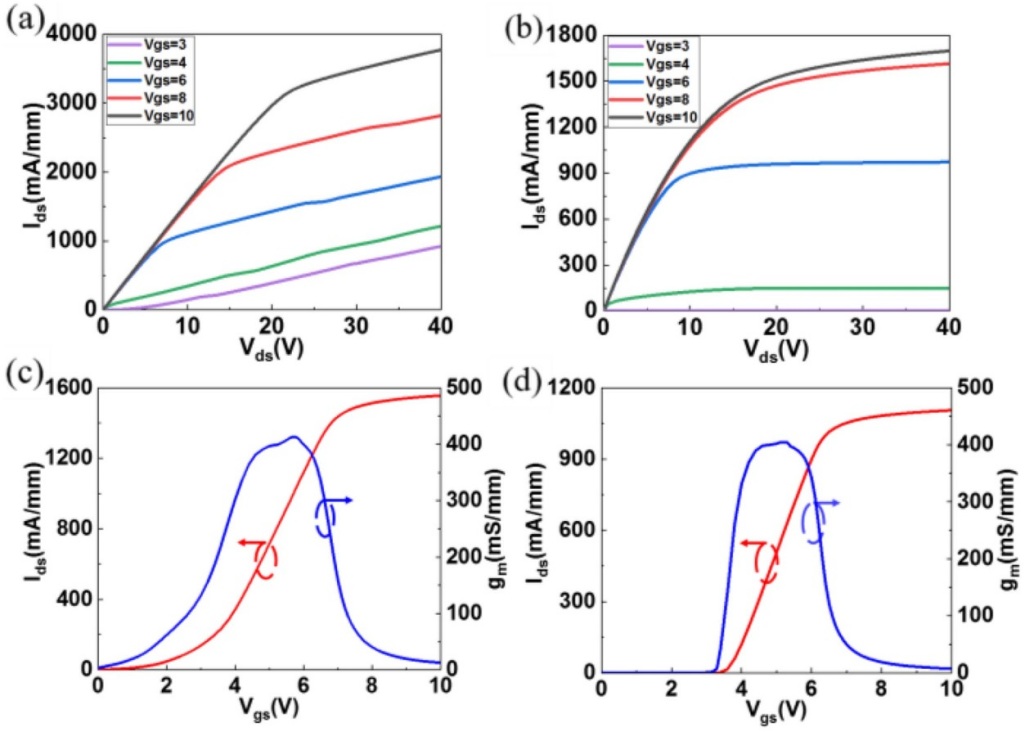

Figure 7. (a) Output characteristics of AlN/β-Ga_2O_3 PIDFET without back barrier layer; (b) output characteristics of AlN/β-Ga_2O_3 PIDFET with GaN back barrier layer; (c) transfer characteristics of AlN/β-Ga_2O_3 PIDFET without back barrier layer under $V_{ds} = 10$ V; and (d) transfer characteristics of AlN/β-Ga_2O_3 PIDFET with GaN back barrier layer under $V_{ds} = 10$ V.

a higher electron density. In addition, a higher transconductance is also obtained in figure 4(e) with a thinner AlN layer, indicating a better gate control.

Figure 6 exhibits the effect of hole concentration of p-GaN gate to the transfer characteristic. The V_{th} extracted from the semi-logarithmic I_{ds}–V_{gs} curves are −0.5, −0.3, 0, 1.2, and 2.6 V for acceptor concentration of 1×10^{17}, 1×10^{18}, 2×10^{18}, 4×10^{18} and 6×10^{18} cm^{-3} respectively. It is obvious that with the increased hole concentration, the V_{th} becomes higher. This trend can be explained by the broadened depletion area in n-type Ga_2O_3 with an increased hole concentration of the p-GaN. Therefore, a higher turn-on voltage, which is desirable in the normally-off operation devices, is needed to form the channel.

3.2. p-GaN gate

In order to further investigate the normally-off operation, we simulated the dependence of the transfer characteristics on different p-GaN gate parameters in terms of the gate length and the hole concentration. Figures 5(a) and (b) show the I_{ds}–V_{gs} curves with different gate length in linear and semi-logarithmic scale, respectively. The threshold voltages extracted from the semi-logarithmic curves (figure 5(b)) are 2.6, 3.3, 3.4 and 3.4 V for the gate length of 0.1, 0.2, 0.3, and 0.4 μm, respectively. The curves of transconductance versus gate voltage with varying gate length are shown in figure 5(c). The maximum values of transconductance extracted from the g_m–V_{gs} are 404.3, 379.6, 364.1 and 348.8 mS mm^{-1} for the gate length of 0.1, 0.2, 0.3, and 0.4 μm, respectively, which suggests that there is a tradeoff between the threshold voltage and the transconductance.

3.3. GaN back barrier layer

The output characteristics of the PIDFET without and with back barrier layer are also compared, and the results are shown in figures 7(a) and (b). From figure 7(a), it is found that the drain current (I_{ds}) is not saturated and the off-state I_{ds} (the purple line) arises significantly, indicating the existence of drain leakage current. In figure 7(b), the drain current is saturated, and a maximum I_{ds} of 1698 mA mm^{-1} is obtained. The off-state drain leakage current can be fully suppressed by the GaN back barrier layer. The detailed principles of the suppression effect of the inserted GaN back barrier were elaborated in section 2.2 as schematically shown in figures 2 and 3. Figures 7(c) and (d) demonstrate the transfer characteristics of the PIDFET without and with the GaN back barrier layer. We can find that the current at the subthreshold region (0 ∼ 4 V in figure 7(c)) is much suppressed by adding the GaN back barrier layer.

4. Conclusion

To unleash the full potential of Ga_2O_3 and III-nitride materials in power device applications and realize a normally-off field-effect transistor, herein, we proposed a normally-off AlN/β-Ga_2O_3 PIDFET via forming a polarization-induced 2DEG channel within the device.

Although early experimental demonstrations of the formation of the III-nitrides/gallium oxide heterostructures have shown the promise for their implementation in III-nitrides/Ga_2O_3-based power electronics, due to the obvious difference in their crystal structures, it is still challenging to grow AlN or Al-rich AlGaN thin films on β-Ga_2O_3 templates or vice versa to form high-quality interfaces [15, 33, 34]. Significant efforts have to be dedicated to the growth optimization. Many growth approaches, such as substrate temperatures, gas flow sequences and rates, film stress control, and initial stage nucleation, are the keys to achieve high-quality epilayers and thus to realize high performance transistors based on III-nitrides/Ga_2O_3 heterostructures in the future [33, 34]. Additionally, due to the narrower bandgap of GaN in comparison with Ga_2O_3, the p-GaN itself has lower critical field which may compromise the breakdown performance in the proposed devices. Other wider bandgap p-type material, for example p-AlGaN layer, may serve better as the gate material, which can be an interesting topic for further investigation.

Nevertheless, in this work, the proposed PIDFET exhibits decent output characteristics, including high source-drain current and high transconductance, which can be attributed to the large 2DEG concentration. We comprehensively investigated the transfer characteristics of the PIDFET with different AlN thickness, p-GaN gate length and doping concentration of p-GaN gate. In order to suppress the off-state drain leakage current and decrease the subthreshold swing, we adopted an AlN/β-Ga_2O_3 PIDFET with a Ga-polar GaN back barrier layer. Our approach could fully leverage the benefits of III-nitrides and Ga_2O_3 materials by taking advantage of the polarization effect at the III-N/Ga_2O_3 interface in the pursuit of future field-effect transistor.

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