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ABSTRACT

The morphology of GaN-on-GaN vertical *p-n* diode devices after reverse-bias electrical stressing to breakdown has been investigated. All failed devices had irreversible structural damage, showing large surface craters that were $\sim 15\text{--}35\ \mu\text{m}$ deep with lengthy surface cracks. Cross-sectional electron micrographs of failed devices showed substantial concentrations of threading dislocations around the cracks and near the crater surfaces. Progressive ion-milling across damaged devices revealed high densities of threading dislocations and the presence of voids beneath the surface cracks; these features were not observed in any unstressed devices. These results should serve as a useful reference for future reliability studies of vertical high-power GaN devices.

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I. INTRODUCTION

Wide bandgap semiconductor materials are of much current interest for many potential applications in power electronics. GaN-based devices are of particular interest because of superior electrical properties such as high critical electric field, low intrinsic carrier concentration, high thermal conductivity, large electron mobility, and high saturation velocity.^{1–5} Vertical GaN devices are preferred to lateral devices for better packaging, higher efficiency, high-current, and high-voltage applications.^{5,6} Conventional GaN devices grown on foreign substrates, such as Si, SiC, and sapphire, have large lattice-mismatch and differences in thermal conductivity. These differences result in GaN devices with high densities of threading dislocations (TDs) ($10^8\text{--}10^{10}\ \text{cm}^{-2}$), which contribute to nonradiative recombination and scattering centers, and limit the performance of electrical and optical devices.⁷ Minimizing the defect density is critical to maximizing device performance since defects affect breakdown voltage, leakage current, device reliability, high-temperature reverse bias, and operating lifetime.⁸ Buffer layers, such as AlN, are commonly used to alleviate lattice-mismatch and differences in thermal expansion between GaN and foreign substrates but these layers add to overall cost and complexity. Recent developments in growth using hydride vapor pressure epitaxy (HVPE) have led to

the availability of freestanding GaN substrates with defect densities lower than $\sim 10^6\ \text{cm}^{-2}$.⁹ Epitaxial GaN-on-GaN layers can be grown with reduced defect density ($<10^4\ \text{cm}^{-2}$) using these bulk substrates, making it feasible to fabricate vertical high-power GaN-on-GaN devices with high breakdown voltages.^{10,11}

Despite the reduced dislocation density in homoepitaxially grown GaN vertical devices, it is still likely that the random presence of TDs is responsible for major reverse-bias leakage and eventual device breakdown. For example, TDs were reported to increase the current leakage path in GaN-based devices,¹² and another study reported that TDs were responsible for breakdown and leakage current.¹³ A study of GaN-based light-emitting diodes (LEDs) grown on sapphire by metalorganic chemical vapor deposition (MOCVD) suggested that leakage current was related to dislocations,¹⁴ and another study suggested that V-defects and associated TDs were responsible for high leakage current.¹⁵ It was also reported that GaN-based blue-light LEDs, grown on freestanding GaN substrates by MOCVD, had suppressed leakage current due to a low TD density.¹⁶ Studies of GaN-on-GaN templates grown by molecular beam epitaxy (MBE) found that reverse-bias leakage occurred at dislocations with a screw component.¹⁷ It was also concluded that screw dislocations were more detrimental for gate leakage than edge or mixed dislocations.¹⁸ A study of

AlGaIn/GaN high electron mobility transistors (HEMTs) correlated increased gate leakage current with defects near gate edges,¹⁹ and HVPE-grown GaN Schottky diodes with micropipe defects were reported to show increased leakage current.²⁰

Despite these results for GaN-based LEDs, as well as lateral HEMTs, a detailed investigation on the effect of dislocations on the performance of vertical GaN *p-n* diodes/devices is lacking. Although it was suggested that TDs caused leakage in vertical diodes grown by MOCVD,²¹ microscopy-based studies do not appear to have been reported. Such studies are critical for further device development since the structural and electrical properties of devices depend sensitively not only on the growth method and the growth conditions but also on the presence of dopants, impurities, and the device structure.¹² This present work has investigated GaN-on-GaN vertical devices that have been electrically stressed to breakdown. A major objective was to gain insight into the failure mechanism and to establish whether surface treatment or surface etching methods during regrowth had any impact on the device failure.

II. EXPERIMENTAL DETAILS

Freestanding 2-in. *c*-plane n^+ GaN substrates with a carrier concentration of $\sim 10^{18} \text{ cm}^{-2}$ were used to grow the GaN device structures using MOCVD. The substrates were provided by Sumitomo Electric Industries Ltd. Nine micrometers of an unintentionally doped (UID) GaN drift layer was grown on the GaN substrates. The surfaces of the UID-GaN layers were treated, as described below, followed by the growth of thin UID-GaN insertion layers ($\sim 50 \text{ nm}$) and overgrowth with Mg-doped *p*-GaN layers with thicknesses of 300–500 nm. The purpose of the insertion layers was to shift the

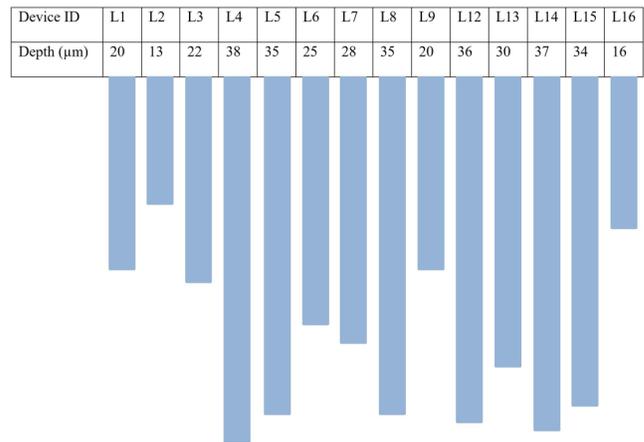


FIG. 2. Schematic illustrating maximum crater depths of Series L devices that had been stressed to failure.

regrowth interfaces (insertion layer/UID-GaN drift layer) well away from the peak electric field in the *p-n* junction depletion region, thus minimizing reverse-leakage current due to any regrowth interface charge contributed by contaminants such as O or Si.

Two sets of devices were investigated in this study, labeled here as A-series and L-series. Both sets were surface-treated (UV-ozone 45 min + HF 5 min + HCl 5 min) before regrowth. The UV-ozone treatment oxidizes the UID-GaN surface, and the following treatments

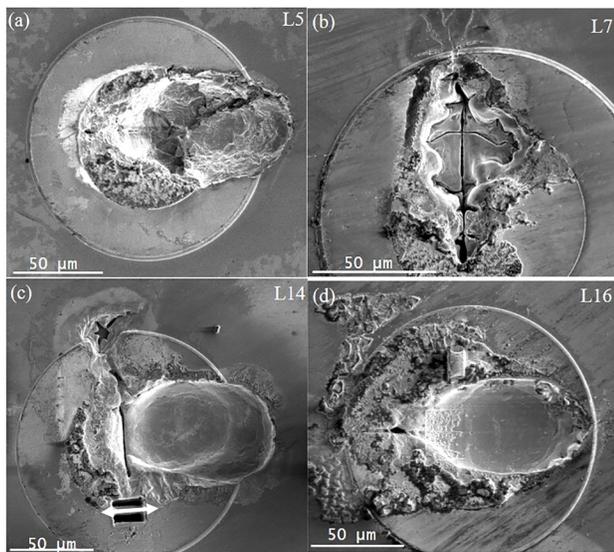


FIG. 1. SEM images showing examples of devices that had been reverse-bias stressed to electrical breakdown, revealing extensive surface damage, including deep craters and wide cracks: (a) Device L5, (b) Device L7, (c) Device L14, and (d) Device L16.

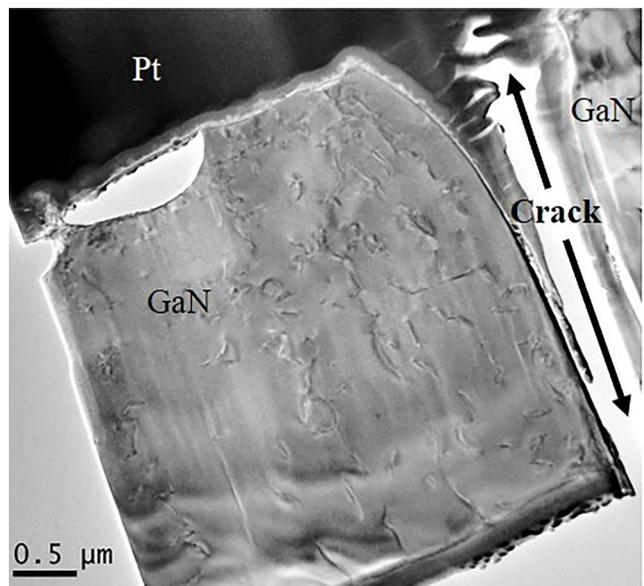


FIG. 3. TEM cross section image of Device L14 from the lift-out location marked in Fig. 1(c), showing the left side of cracks with many dislocations more concentrated toward the crater surface and crack.

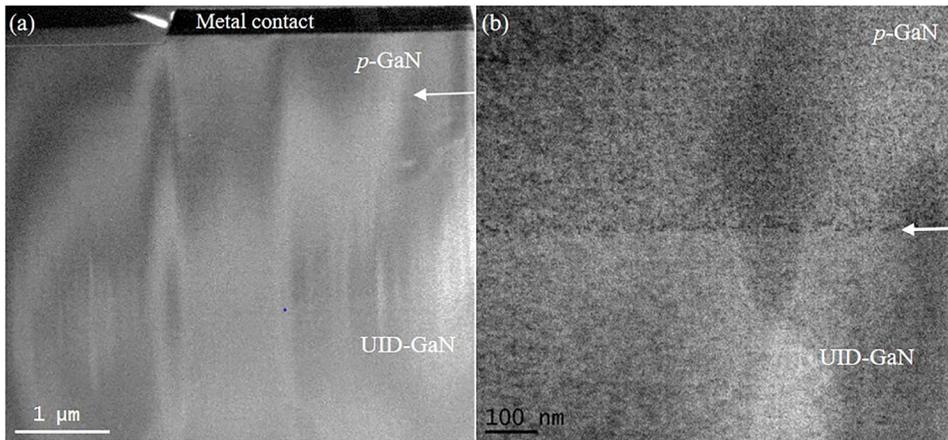


FIG. 4. (a) TEM cross-sectional image of unstressed devices showing the absence of dislocations over the entire lift-out sample and (b) enlargement of the *p*-GaN/insertion layer/UID-GaN region showing no surface-treatment damage or defects.

with HF and HCl are intended to remove surface contaminants. In addition, the A-series devices were etched using inductively coupled plasma (ICP) dry-etching. The ICP dry-etching procedure was a sequence of etching steps intended to remove the surface layer and minimize etch damage, which was achieved by employing four consecutive etching steps with decreasing RF-power (70, 35, 5, and 2 W).²²

More details about the growth and treatment procedures can be found elsewhere.²³ The L-series devices showed breakdown voltages in the range of 200–750 V with typical reverse-leakage current densities of 10 A/cm² at breakdown, whereas the A-series devices exhibited substantially higher breakdown voltages of 1070–1270 V with typical reverse-leakage current densities of 4 A/cm² at breakdown.

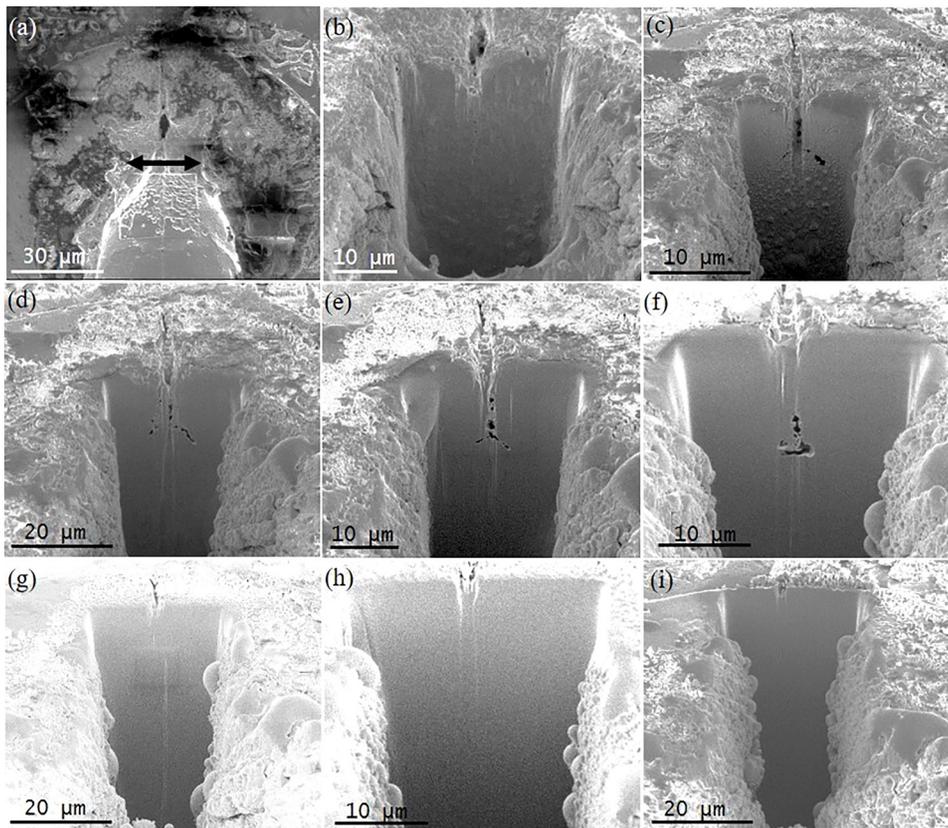


FIG. 5. Series of SEM images of Device L16, showing progressive cross-sectional milling across area of 30 μm (length) × 25 μm (depth): (a) plan-view image showing the location where milling started (black double-headed arrow); (b) cross-sectional image after 5 μm of milling, showing the presence of voids right below the surface crack; (c) cluster of voids; (d) voids extending from the surface just below crack to ~16 μm deep; (e) voids and TDs; (f) presence of TD clusters all over area; (g) and (h) TDs extending from the substrate; and (i) milled almost to the edge of device.

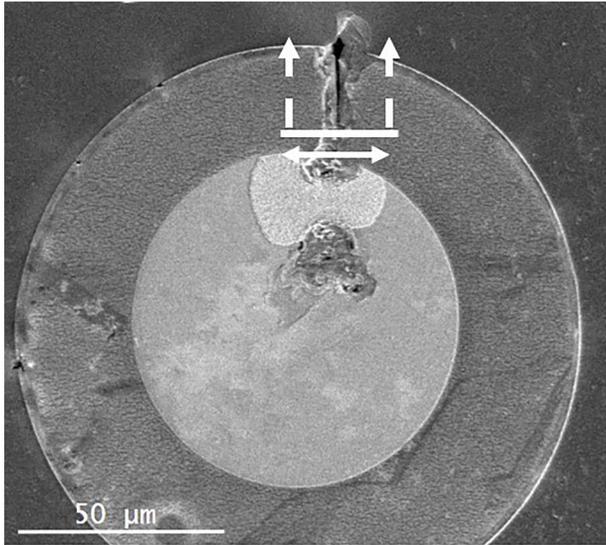


FIG. 6. Plan-view SEM image of Device A1 after reverse-bias breakdown at ~ 1.27 kV, showing surface pits and crack. White arrowed lines indicate the location of cross-sectional milling and double-arrowed line indicates the location of TEM lift-out.

Samples suitable for cross-sectional observation by transmission electron microscopy (TEM) were prepared by focused-ion-beam (FIB) milling using an FEI NOVA 200 dual-beam system with initial thinning done at 30 keV and final thinning done at 5 keV. Scanning electron micrographs were also recorded with the FEI NOVA 200 during progressive milling across the surface craters that were observed in failed devices. A Philips-FEI CM-200 FEG transmission electron microscope (TEM) operated at 200 keV was used for structural imaging. All TEM images were taken at the [1100] zone axis. High-resolution images were taken using phase contrast imaging without an objective aperture. Low-magnification and medium-magnification images were taken using an objective aperture for better contrast.

III. RESULTS

Examples of plan-view SEM images of devices L5, L7, L14, and L16 after they were reverse-bias stressed to breakdown are shown in Fig. 1. This set of devices had been regrown with an insertion layer of 250 nm, followed by another 500 nm *p*-GaN, after the surface layer of the original UID-GaN had been chemically treated. All stressed devices showed extensive, craterlike surface pits, and most also showed evidence for lengthy cracks extending across parts of the craters and even outside the device region in some cases. Sixteen devices were stressed to breakdown and all 16 showed similar craterlike surface damage with varying crater depths. The measured depths of these craters ranged from 13 to 38 μm , as shown schematically in Fig. 2.

Lift-out with the FIB was performed across the crack on Device L14, as indicated by the arrow in Fig. 1(c), and the corresponding TEM image is shown in Fig. 3. This cross-sectional image reveals a high density of dislocations along the left side of the crack, which appear to be more concentrated toward the GaN surface and adjacent to the crack. For comparison, Fig. 4(a) shows a cross-sectional TEM image of an unstressed device, where the white arrow indicates the position of the interface between *p*-GaN and the insertion layer. No dislocations or cracks are visible and no structural damage between the insertion layer and the UID-GaN layer due to surface treatment can be observed. The enlargement in Fig. 4(b) shows the *p*-GaN/insertion layer/UID-GaN area where there are no visible defects or surface damage, although the top *p*-GaN layer shows evidence for Mg precipitates.

In order to appreciate the full extent of defect formation in the failed devices, Device L16 was progressively milled in cross section across the surface crater and then repeatedly imaged *in situ* with the SEM after another roughly 5 μm had been milled away. Figure 5(a) shows a plan-view SEM image of the original device after failure before commencement of trenching. Milling started at the top of crater at the position indicated by the arrow and then proceeded progressively upward. Figures 5(b)–5(h) are a series of SEM images showing the progression of this milling over an area of roughly 30 \times 25 μm^2 . Figure 5(b) reveals a collection/cluster of voids that are present in the GaN substrate beneath the crack. Figures 5(c)–5(e) show parts of the same void cluster after the additional material, about 5 μm at a time, had been removed. Figures 5(c)–5(f) show a

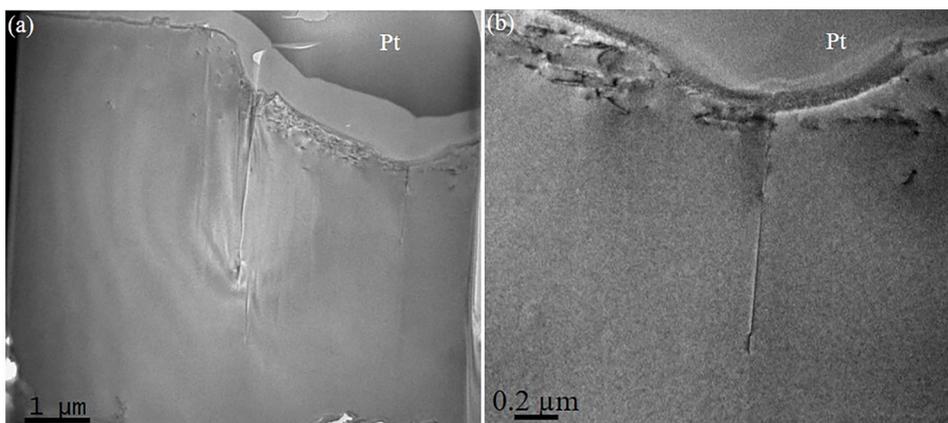


FIG. 7. Cross-sectional TEM images of Device A1 lift-out across the surface crack from location marked with double-arrowed line in Fig. 6: (a) low-magnification image showing large 4- μm -deep crack, smaller cracks, and the presence of dislocations concentrated near the cracks and surface and (b) high-magnification image showing small 2- μm -deep crack and surrounding defects.

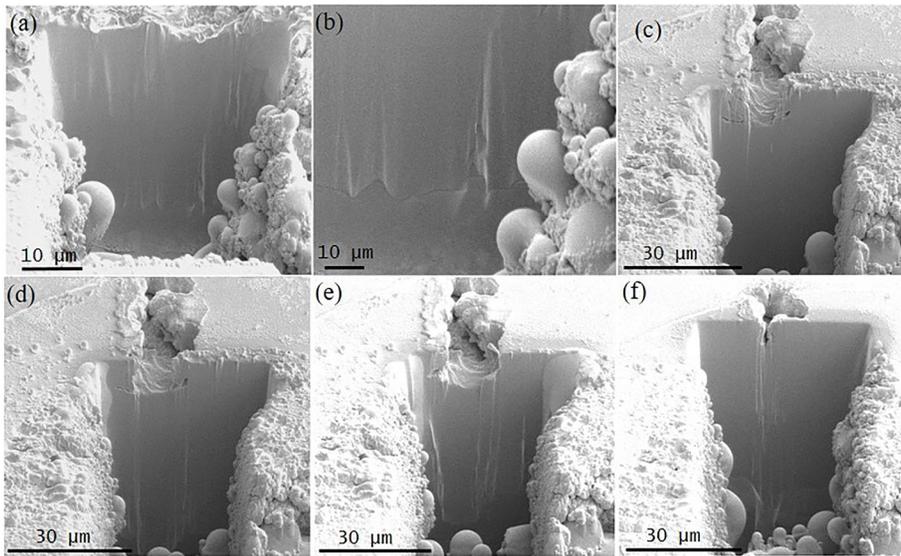


FIG. 8. Sequential series of SEM images of Device A1 after progressive cross-sectional milling across area of $40\ \mu\text{m}$ (length) \times $25\ \mu\text{m}$ (depth) from the location marked with arrowed white lines in Fig. 6: (a) TDs all over milled area; (b) high-magnification image focused on TD that extended $\sim 49\ \mu\text{m}$ down from the crater surface; (c) voids concentrated nearer to cracks; (d) surface crack that appears to be $\sim 15\ \mu\text{m}$ deep extending into the device; (e) TDs near and away from cracks and extending deep from the substrate; and (f) milling stopped at the edge of device and surface crack extending outside devices is still observed.

cluster of threading dislocations at the center of image, right below the crack, and away from the surface crack. Figure 5(e) shows a threading dislocation extending from the crater surface to deep within the substrate over a vertical distance of almost $80\ \mu\text{m}$.

In addition to the chemical etching used for the L-series, Devices A1 and A2 of the A-series were ICP dry etched, followed by growth with $50\ \text{nm}$ of the GaN insertion layer and overgrowth with $500\ \text{nm}$ of *p*-GaN. Device A1 suffered electrical breakdown at a reverse bias of $\sim 1.27\ \text{kV}$. It was then observed for surface anomalies, as shown by the SEM image in Fig. 6. The surface shows pits near the center of the circular contact with a long crack that extends across part of the device to outside the device area. The crater and the crack surface morphology appear similar to that observed for the L-series devices despite the considerable difference in breakdown voltages.

A cross-sectional sample suitable for TEM observation was lifted-out across the visible crack of Device A1, as marked in Fig. 6 by the double-headed arrow. Figure 7 shows corresponding TEM images. Figure 7(a) reveals that the entire top surface region here is riddled with dislocations, not unlike the L-series devices, and a crack is also visible that penetrates more than $4\ \mu\text{m}$ from the crater surface. Figure 7(b) from an adjacent area shows another crack that extends almost $2\ \mu\text{m}$ downward from the crater surface. Dislocations here are concentrated close to the crack and along the top surface, as clearly visible in Fig. 7(b). The GaN top surface is not flat/even because of the irregular loss of surface material that occurred during the device breakdown.

Figure 8 shows a sequence of cross-sectional SEM images of Device A1 after progressive milling had been done along the direction indicated by the arrowed lines in Fig. 6. Figures 8(a) and 8(c) reveal the presence of TDs all across the milled area, while Fig. 8(b) shows a TD that extends almost $49\ \mu\text{m}$ downward from the crater surface. Figures 8(d) and 8(e) show that the surface crack is almost $15\ \mu\text{m}$ deep, and that TDs are present everywhere. For comparison, Fig. 9 shows TEM images of the equivalent Device A2, which was not subjected to any electrical tests. Figure 9(a) shows that no dislocations or

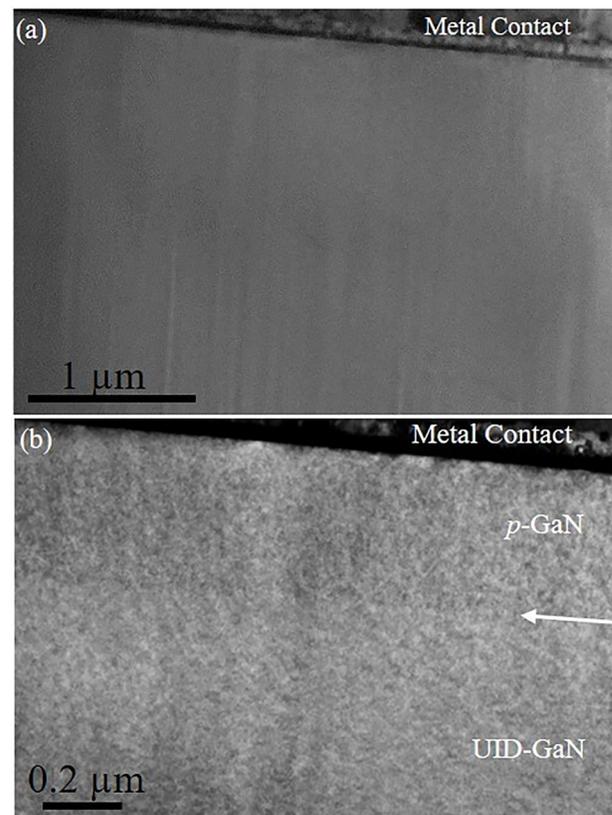


FIG. 9. Cross-sectional TEM images of Device A2 which was not subjected to any electrical tests: (a) low-magnification image shows no cracks or dislocations and (b) high-magnification image of the *p*-GaN/insertion layer/UID-GaN area shows no visible etch damage or defects.

cracks are present in the lifted-out area. The enlargement in Fig. 9(b) shows the *p*-GaN/insertion layer/UID-GaN area, and no etching-based damage or structural defects are visible.

IV. SUMMARY

This paper described the irreversible structural changes observed in two sets of GaN-on-GaN high-power devices after they had been reverse-biased to the point of electrical breakdown. Surface-treated devices (Series L) developed deep craters and lengthy cracks when failure occurred. The craters extended across much of each failed device and had depths of tens of micrometers. The failed devices also showed the presence of cracks, clusters of voids, and TDs under the craters. These cracks extended typically about 6–15 μm downward. The voids were present in the substrate region, whereas TDs were present across entire devices extending deep into the substrate. Devices that had been etched and then overgrown (Series A) showed similar morphology after failure, although their breakdown voltages were considerably higher. Cracks were again observed on the cratered surfaces of the failed devices, while cross-sectional TEM images showed the formation of threading dislocations that were concentrated close to the cracks and near the crater surfaces. Similar dislocations were never observed in unstressed devices subjected to identical etch-regrowth treatment. The presence of pre-existing defects in devices before regrowth does not seem to be an important factor in device failure since the Series L and Series A devices were grown on similar substrates, but they had significantly different breakdown voltages. The lower breakdown voltages for the surface-treated devices can most likely be attributed to surface oxidation during the UV-ozone treatment. Overall, these results provide highly useful information about the reliability of vertical power electronics and should contribute to the design of better future devices.

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