GaN Vertical-Channel Junction Field-Effect Transistors With Regrown p-GaN by MOCVD

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***Abstract*— We report an experimental demonstration of GaN-based vertical-channel junction field-effect transistors (VC-JFETs). A p-GaN regrowth by metalorganic chemical vapor deposition (MOCVD) and a subsequent self-planarization process were developed to fabricate the GaN VC-JFETs. Fin-like channel regions were patterned by electron beam lithography (EBL) and aligned to *m*-plane or *a*-plane. The electrical properties of lateral and vertical p-n junctions were characterized to verify the effectiveness of the p-GaN regrowth. Both VC-JFETs with *m*-plane and *a*-plane channels show decent gate modulation. We further discussed important factors that may affect the device performance including interfacial impurities and nonuniform acceptor distribution. This work highlights the successful demonstration of GaN VC-JFETs and lateral p-n junctions by an etch-then-regrow process, providing valuable information and reference for the further development of GaN power electronics.**

***Index Terms*— Gallium nitride, junction field-effect transistor (JFET), p-GaN regrowth, selective area doping.**

I. Introduction

THE III-nitride semiconductors have attracted considerable attention for various applications in optoelectronics [1], [2], photonics [3], [4], and electronics [5]. Recently, GaN-based power electronics have been extensively researched due to GaN's large bandgap (E_g), high breakdown electric field (E_b), and large Baliga's figure of merit (BFOM). With the commercialization of high-quality bulk GaN substrates, GaN vertical devices have become prominent candidates for the next-generation efficient power electronics, capable of achieving high currents and high breakdown voltages (BVs) with smaller chip area and better thermal management [6]–[8].

Manuscript received March 6, 2020; revised April 21, 2020, May 27, 2020, and July 14, 2020; accepted July 15, 2020. Date of publication August 5, 2020; date of current version September 22, 2020. This work was supported in part by the ARPA-E PNDIODES Program monitored by Dr. Isik Kizilyalli under Grant DE-AR0000868, in part by the NASA HOTTech Program under Grant 80NSSC17K0768, and in part by NanoFab through the NSF under Contract ECCS-1542160. The review of this article was arranged by Editor Y. Cao. *(Corresponding author: Yuji Zhao.)*

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Digital Object Identifier 10.1109/TED.2020.3010183

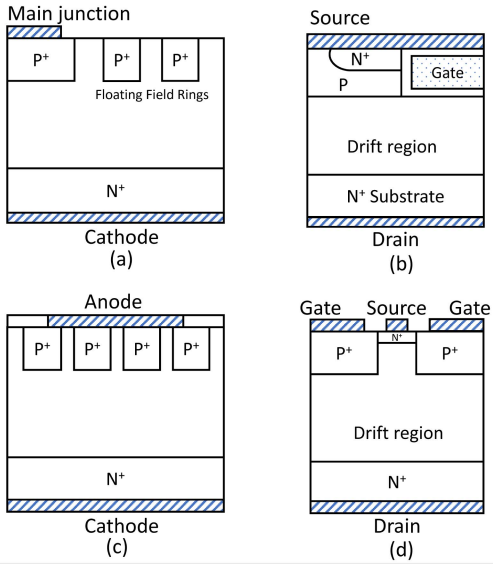

Fig. 1. Schematics of advanced GaN power devices and structures enabled by selective area doping. (a) JTE. (b) U-MOSFETs. (c) JBS diodes. (d) JFETs.

However, selective area doping still remains one of the most critical hurdles for GaN power electronics [9]–[12], which hinders the demonstration of many advanced GaN power devices and structures, such as junction termination extension (JTE), U-shape metal–oxide–semiconductor field-effect transistors (U-MOSFETs), junction barrier Schottky (JBS) diodes, and junction field-effect transistors (JFETs) (see Fig. 1). Compared with the immature ion implantation and thermal diffusion methods, etch-then-regrow is still regarded as one of the most promising methods to realize selective area doping in GaN [13]–[16]. Currently, there are still some challenges in etch-then-regrow progress. In an etched trench, the regrowth interfaces are composed of both polar ***c***-plane and nonpolar planes (***a***- or ***m***-plane) that have very different atom arrangements and dangling bond densities, resulting in anisotropic material and electrical properties. For example, the nonpolar planes are more susceptible to contamination and impurity incorporation than the ***c***-plane (Ga-face) due to the presence of nitrogen atoms [17]. Another challenge is the nonuniform Mg or acceptor distribution in the trench regrowth. Liu *et al.* [18] reported that the sidewall of Mg-doped p-GaN grown over a mesa structure was acceptor-deficient, which led to lower hole concentrations on nonpolar sidewall facets.

Furthermore, the use of common dielectric growth masks, such as SiO_2 and Si_3N_4, during regrowth can result in Si diffusion into p-GaN, giving rise to n-type conductivity instead of p-type. In this work, the etch-then-regrow utilizes a maskless blanket regrowth process to ensure the regrown p-GaN has p-type conductivity. Although some regrown GaN p-n diodes have been demonstrated by blanket regrowth on planar surfaces [19], the reports on GaN-regrown devices in trenches or fins, such as GaN JFETs, are still scarce.

Recently, the FinFET concept has enlightened vertical power transistors based on wide bandgap (WBG) and ultrawide-bandgap (UWBG) semiconductors [20]. Two types of enhancement-mode vertical GaN field-effect transistors with fin-like channels have been proposed: Fin MOSFETs and vertical-channel junction field-effect transistors (VC-JFETs). Fin MOSFETs use MOS gates to pinch off the fin channel, whereas VC-JFETs rely on lateral p-n junction gates to modulate the fin channel. Both types of devices have the potential to realize kilovolts BVs [21]. In addition, lateral p-n junctions are also building blocks for more complicated bipolar GaN power devices [7]. Sun *et al.* [22] demonstrated GaN Fin MOSFETs with a threshold voltage of 1 V and specific ON-resistance ($R_{ON,sp}$) of 0.36 $m\Omega \cdot cm^2$ (normalized by the active fin area) and 800-V blocking voltage. $R_{ON,sp}$ was 3.24 $m\Omega \cdot cm^2$ if normalized by the total device area. Zhang *et al.* [23] further demonstrated GaN fin MOSFETs with BV of 1.2 kV and $R_{ON,sp}$ of 0.2 $m\Omega \cdot cm^2$ (normalized by the active fin area). $R_{ON,sp}$ was 1 $m\Omega \cdot cm^2$ if normalized by the total device area. Zhang *et al.* [23] also demonstrated large-area devices with ON-current of 5 A and $R_{ON,sp}$ of 2.1 $m\Omega \cdot cm^2$ (normalized by the total device area). The only experimentally reported VC-JFETs by Kotzea *et al.* [24] showed very weak gate modulation effects with a large leakage and a drain current ON/OFF ratio of less than 2. The poor device performance is partly due to limited understanding of nonideal effects during regrowth on fin-like channels.

In this work, we designed and fabricated the GaN VC-JFETs on bulk GaN substrates by metalorganic chemical vapor deposition (MOCVD). The p-GaN gates were regrown on GaN epilayers with fin-like channels patterned by electron beam lithography (EBL). A maskless blanket regrowth and a subsequent self-planarization process were applied to define the p-GaN gate regions. GaN VC-JFETs with a decent ON/OFF ratio of ~100 and very high transconductance of over 600 S/cm^2 were achieved, which are considerable improvements over previous reports. The nonideal factors that limit the device performance during regrowth were also analyzed by secondary ion mass spectroscopy (SIMS) and cathodoluminescence (CL).

II. Device Structure and Fabrication

The device epilayers were grown by MOCVD where trimethylgallium (TMGa) served as the Ga precursor and ammonia (NH_3) was the source for nitrogen. The carrier gas was hydrogen (H_2). Fig. 2 shows the growth and fabrication process of the GaN VC-JFETs. A 4-μm-thick unintentionally doped (UID) GaN was homoepitaxially grown on heavily doped bulk GaN substrates. The background electron

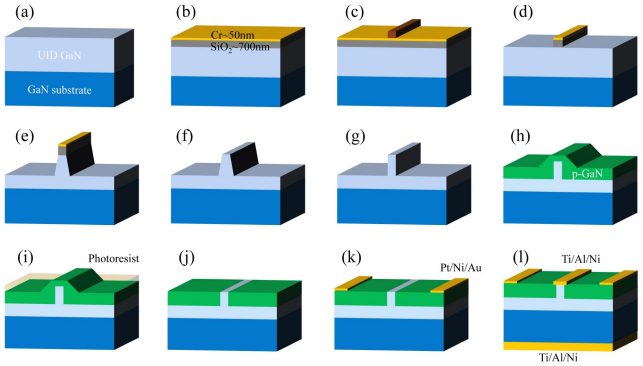

Fig. 2. Fabrication process of the VC-JFET. (a) Epilayer growth. (b) Cr and SiO_2 hard masks deposition. (c) E-beam lithography. (d) ICP etching to define hard masks. (e) Two-step ICP etching. (f) Hard masks removal. (g) TMAH wet etching. (h) p-GaN regrowth. (i) Photoresist assisted planarization. (j) Top p-GaN etching. (k) Gate metal contacts deposition. (l) Source and drain metal contacts deposition.

density was estimated to be ~10^{16} cm^{-3} by capacitance–voltage (C–V) measurement. Cr (50 nm)/SiO_2 (700 nm) were deposited as hard masks for fin patterns that were transferred by EBL. The chlorine- and fluorine-based reactive ion etchings (RIEs) were used to etch Cr and SiO_2 hard masks, respectively. To improve the regrowth surface, the fins were formed by a two-step inductively coupled plasma (ICP) etching: a 6-min high-RF-power fast etching (~280 nm/min) and a 3-min low-RF-power slow etching (~20 nm/min). Our previous results showed that low RF power ICP etching can improve the performance of regrown planar p-n junctions [25]. The hard mask residuals (Cr and SiO_2) were removed by Cr etchant and hydrofluoric (HF) acid. The samples were then dipped in 75 °C 25% hot tetramethylammonium hydroxide (TMAH) for 5 min to further recover etching damages created by ion bombardments during ICP etching. The samples were then immersed in piranha for 15 min to further remove possible organic contaminants [26]. The samples were then treated by UV-ozone for 1 h, followed by a buffered oxide etch (BOE) and 10% hydrochloric (HCl) acid for 5 min, respectively, to remove surface charges. Finally, the thoroughly cleaned samples were immediately reloaded into the MOCVD chamber for p-GaN regrowth. A 1 μm p-GaN with an Mg concentration of 10^{19} cm^{-3} was regrown on the sample using bis(cyclopentadienyl)magnesium (Cp_2Mg) as the Mg precursor. After the regrowth, acceptor activation of the regrown p-GaN was conducted at 700 °C for 20 min in a nitrogen environment. A photoresist-based planarization process was used to selectively etch away the p-GaN on top of the fin and expose n-GaN for source contacts. Gate electrodes were formed by Pd/Ni/Au (30/20/100 nm) by electron beam evaporation and then annealed at 450 °C for 5 min in a nitrogen ambient. Finally, the source and drain electrodes Ti/Al/Ni (30/100/30 nm) were deposited by electron beam evaporation.

The VC-JFET devices with fins aligned to either ***a***-plane or ***m***-plane were fabricated. Fig. 3(a) shows the schematic of the GaN crystal planes. The alignment direction relative to the orientation flat (OF) is shown in Fig. 3(b). The wet etching of TMAH in GaN is strongly anisotropic, which results in different sidewall profiles for the two different

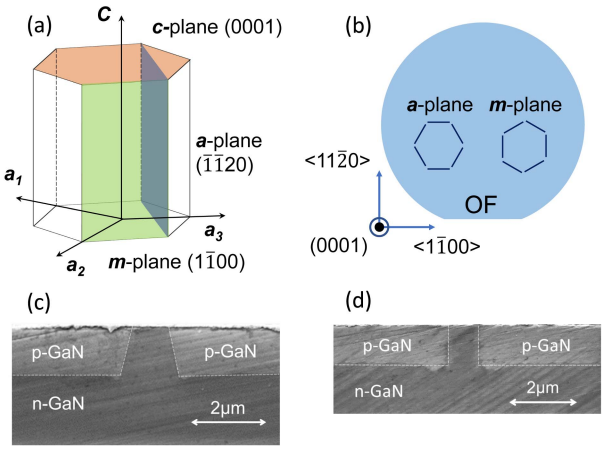

Fig. 3. (a) Crystal planes in GaN wurtzite structure. (b) Schematics of the fin alignment direction. SEM cross-sectional images of the VC-JFETs in (c) ***a***-plane and (d) ***m***-plane.

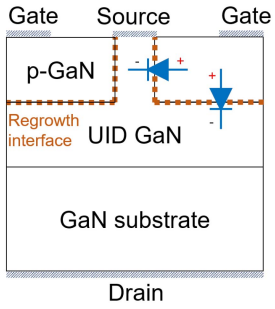

Fig. 4. Schematics of the cross section of GaN VC-JFETs.

crystal orientations [27]. The device aligned to the ***m***-plane in Fig. 3(d) shows a narrower and more vertical fin than that the device aligned to ***a***-plane in Fig. 3(c).

III. Results and Discussion

A. Regrowth Verification

In the GaN VC-JFETs, two types of p-n junctions were formed by the p-GaN regrowth: the lateral and vertical p-n junctions, as shown in Fig. 4. The former was the junction between the gate and the source, and the latter was the junction between the gate and the drain. The junctions shared the same gate electrode that was attached to p-GaN. The n-contacts for the lateral and vertical p-n junctions are formed on the exposed fin ($\sim$960 μm^2) and the backside of the wafer, respectively. The currents were normalized by the gate electrode area, which is $\sim 1 \times 10^5$ μm^2. The current–voltage (I–V) characteristics of the two p-n junctions were measured by a Keithley 2410 source meter. Fig. 5(a) and (b) shows the representative I–V curves of the vertical and lateral p-n junctions, respectively. Similar forward rectifying characteristics with an ON/OFF ratio of $\sim 10^5$ were observed for both junctions. At forward bias, strong electroluminescence (EL) was observed, which indicates that the p-GaN regrowth was effective. The turn-on voltages, as extracted from linear extrapolation, were 3.4 and 3.1 V in the vertical and lateral p-n junctions, respectively. This larger turn-on voltage of the vertical p-n junction is likely due to the thicker n-GaN layer in the vertical direction. The two junctions showed abnormal ideality factors of over 4. This is likely caused by the regrowth

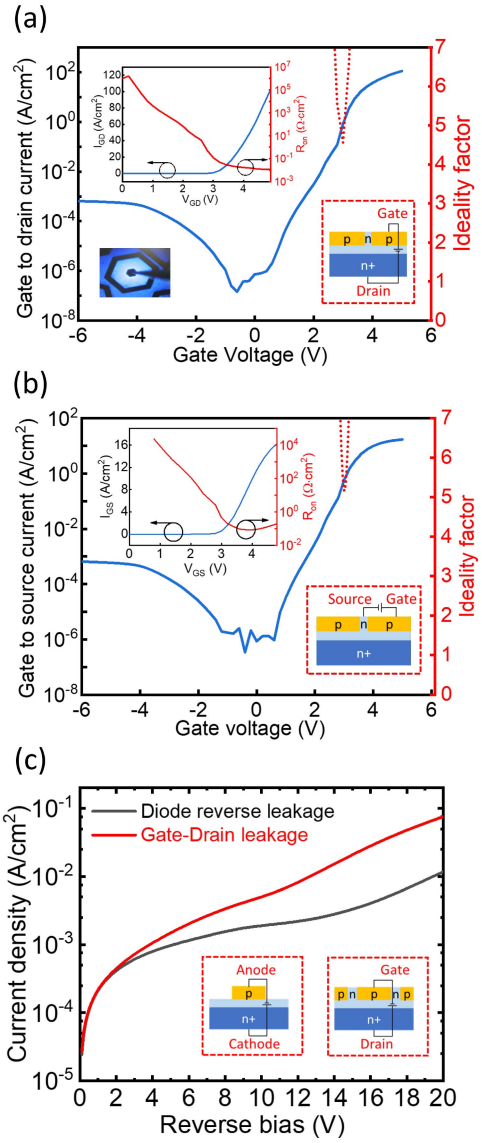

Fig. 5. (a) I–V curves for the vertical p-n junctions between the gate and the drain. (b) I–V curves for the lateral p-n junctions between the gate and the source. The insets show schematics of the p-n junctions in GaN VC-JFETs. (c) Reverse leakage current of a planar diode and a p-n junction between the gate and the drain.

process since defects, etching damage, and impurities can serve as nonradiative recombination centers at the regrowth interfaces, thus increasing ideality factors. The lateral and vertical p-n junctions show similar leakage currents, which are further compared with previous reports. The leakage currents in this work are comparable to the reported regrown p-n junctions and not surprisingly larger than as-grown vertical p-n diodes [28]. In this work, the p-GaN layer was directly regrown on UID-GaN. It was reported that introducing an undoped insertion layer may move the surface impurities away from p-GaN and reduce the leakage in the regrown p-n junctions [25], which is an on-going topic.

To understand leakage paths for the regrown p-n junctions, the reverse leakage characteristics of a planar diode (without fins) and a vertical p-n junction between the gate and the drain (with fins) on the same wafer are compared in Fig. 5(c). Both p-n diodes show larger leakage currents compared with

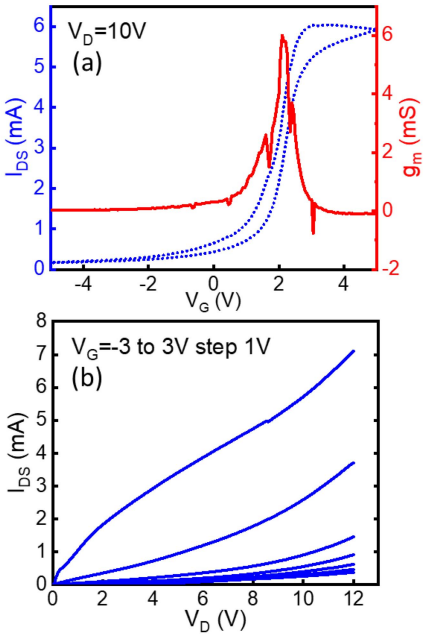

Fig. 6. Device electrical properties. (a) Representative I_D–V_{GS} transfer characteristics in a linear scale. (b) Representative I_D–V_{DS} output characteristics.

as-grown diodes. The discrepancy between the two diodes becomes larger at higher reverse bias. This suggests that both nonpolar and polar regrowth interfaces contribute to the leakage current. The total leakage is the superposition of leakage currents from all etched surfaces. The ***c***-plane interface may be dominant at a low bias (<2 V), and the leakage current through nonpolar planes increases with increasing reverse bias. The leakage currents continue to increase after 10 V with no sign of saturation.

B. VC-JFET Characteristics

The transistor characteristics were measured by a Keithley 4200 SCS parameter analyzer. The effective area for the source region is 960 μm^2, consisting of six fins each with an area of 1 μm × 160 μm. The total device area, including the source/gate electrode areas, is $\sim 2.5\times10^5$ μm^2. Fig. 6(a) shows the transfer characteristics of the VC-JFET with fins aligned to ***m***-plane. At a drain voltage of 10 V, the ON/OFF ratio is ~100, which is much higher than the previous report (which is less than 2) [24]. As the gate voltage increased to 2.2 V, the gate current begun to increase due to the turn-on of the gate to source p-n junction, and as a result, the drain current slightly decreased. A hysteresis of ~0.4 V was observed in the I_D–V_{GS} transfer curve due to charges at the regrowth interface.

Fig. 6(b) shows the output I_D–V_{DS} family curves. Gate modulation was obtained, but no current saturation was observed in the VC-JFET mainly due to gate leakage. The drain current density reached 740 A/cm^2 with an $R_{ON,sp}$ of 10.5 m$\Omega\cdot$cm^2 (normalized by the fin area) at a V_G bias of 3 V and V_{DS} bias of 12 V. The ON-resistance normalized by the total device region is 2.8 $\Omega\cdot$cm^2. Since nonalloyed contacts for the source and the drain were used, thermal annealing may further decrease the ON-resistance.

Typical OFF-state I_D, I_G–V_D curves of the GaN VC-JFETs are shown in Fig. 7. The gate current was mainly the

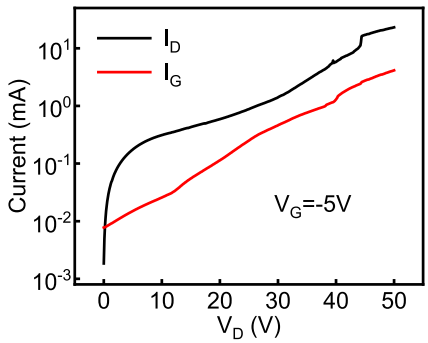

Fig. 7. Representative OFF-state characteristics of the VC-JFETs.

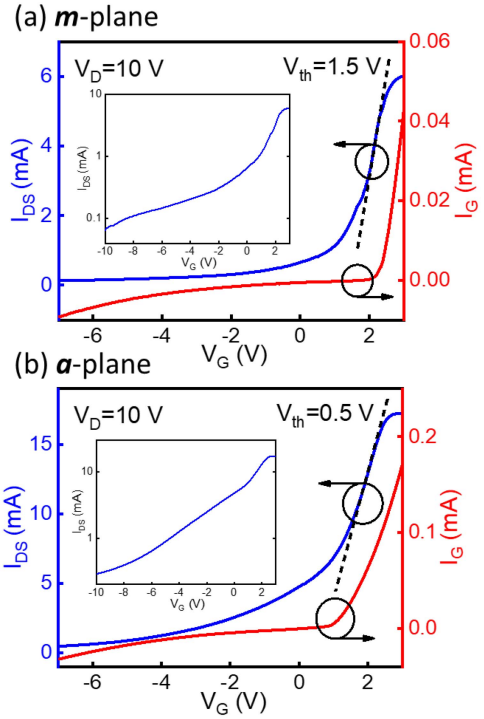

Fig. 8. Transfer characteristics of VC-JFETs aligned to different crystal orientations: (a) ***m***-plane and (b) ***a***-plane.

superposition of leakage current from both lateral and vertical p-n junctions. The drain current consists of leakage current from vertical p-n junctions and the leakage current induced by the weak pinch-off effects of lateral p-n junctions. The drain current is around ten times higher than the gate current, indicating the drain leakage contributed to the main leakage in drain current at the OFF-state. The drain current broke down at 45 V, while no breakdown was observed at the gate. These results suggest that the OFF-state characteristics of this device are primarily limited by weak pinch-off effects of the lateral p-n junctions.

C. Comparison of a-plane and m-plane Devices

Fig. 8(a) and (b) compares the transfer characteristics of the VC-JFETs aligned to ***m***-plane and ***a***-plane, respectively. The peak transconductances are 625 and 916 S/cm^2 (normalized by fin areas) in ***m***-plane and ***a***-plane devices, respectively, [29]–[33]. The threshold voltages (V_{th}) are determined by the following method: first, the point of maximum transconductance on the I_D–V_{GS} curve was found, and the

maximum slope was extrapolated to $I_{DS} = 0$ to find the x-axis intercept. The ***m***-plane and the ***a***-plane devices showed turn-on voltages at ∼1.5 and ∼0.5 V, respectively.

The ***a***-plane device showed higher ON-current compared to the ***m***-plane. This discrepancy is likely due to nonalloyed source contacts. The UID-GaN was treated with ICP etching to created donor-like surface defects to facilitate drain contacts [34]. While different surface conditions before electrode deposition may lead to nonuniform contact resistance in different devices, the gate leakage in the ***a***-plane devices is around ten times higher than that of the ***m***-plane devices. This difference in gate leakage is likely related to different crystal orientations. It has been shown that ***m***-plane sidewalls are much smoother than the ***a***-plane after TMAH treatment [35]. A recent study also shows that GaN vertical MOSFETs with trenches aligned to the ***m***-plane present better performance than ***a***-plane [33]. It is possible that the defect and impurity level at ***m***-plane could be lower than ***a***-plane after TMAH treatment, resulting in lower gate leakage.

D. Nonideal Factors in Regrowth

Interfacial impurities, such as silicon (Si) and oxygen (O), have been shown to strongly affect GaN regrown p-n diodes [36], [37]. In our previous study under the same growth condition, it was observed that there were high levels of positively charged donors at the regrowth interface. These donors were attributed to Si (∼10^{19} cm^{-3}) and O (∼10^{17} cm^{-3}) at the ***c***-plane according to the SIMS results [28]. Such high levels of impurities were also observed at ***m***-plane regrown interfaces [38]. Using electron holography, the electrostatic potential profile at the regrowth interface was obtained. The energy band diagram showed a large band bending at the regrowth interface. This indicates the formation of a p^+/n^+ tunneling junction at the regrowth interface. n^+-GaN is due to a high concentration of Si and O impurities acting as shallow donors, and the p^+ doping at the regrowth interface is likely due to Si-Mg and/or O-Mg codoping effects. Research has shown that the overlapping of Mg and Si/O at the interface region can enhance the hole concentration up to two orders of magnitude [39]. The formation of tunneling junctions at the regrowth interface is likely to be responsible for the large leakage, premature breakdown in regrown p-n junctions, and weak pinch-off effect of the lateral p-n junctions. More in-depth analysis of the effects of impurities and electron holography can be found in [40]. Recently, Xiao *et al.* [41] reported that Mg preflow before p-GaN growth can compensate for the interfacial Si/O impurities. This method is promising in enhancing the regrown junction blocking capabilities.

Another factor limiting the device performance is the nonuniform distribution of acceptors in GaN epilayers grown on fin structures. CL spectroscopy was used to study the optical properties of p-GaN in VC-JFET devices. The CL was carried out in a JEOL 6300 scanning electron microscope. The electron beam current used in this study was 100 pA, and the acceleration voltage was 7 kV. CL mappings were obtained by recording the spatial variation of luminescence intensity over an area at a certain wavelength. Fig. 9 shows the secondary electron (SE) images and CL mappings at 3.25 and 2.9 eV of

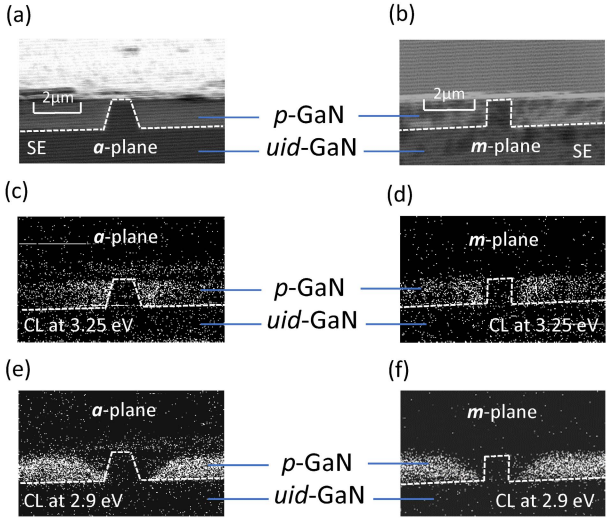

Fig. 9. Cross-sectional view of the VC-JFETs devices: SE images of devices aligned to (a) ***a***-plane and (b) ***m***-plane. Monochromatic CL images at 3.25 eV for devices aligned to (c) ***a***-plane and (d) ***m***-plane. Monochromatic CL images at 2.9 eV for devices aligned to (e) ***a***-plane (f) ***m***-plane.

m- and ***a***-plane devices. According to [18], 2.9-eV emission intensity in CL can be used as an indicator of acceptor concentrations. The higher the CL intensity at 2.9 eV, the higher the acceptor concentration. It is clear in Fig. 9(e) and (f) that weaker intensity was observed on the sidewalls of the fins, indicating that the p-GaN grown on the sidewall of the fins had lower acceptor concentration. This can adversely impact the device performance since the fin channel will be more difficult to be pinched off due to weaker depletion effects in the channel at lower acceptor concentrations. This could make it more difficult to achieve enhancement mode in VC-JFETs. The interface between acceptor-deficient p-GaN and normal p-GaN makes a 45° angle with the basal plane in both ***m***- and ***a***-plane devices. This indicates that this phenomenon is not related to crystal orientations and possibly due to regrowth conditions and/or surface treatment.

All the aforementioned nonideal factors indicate that device regrowth with trenches is much more complicated and difficult than regrowth on planar surfaces. To achieve complete pinch-off in channels, the tunneling junctions at the regrowth interface must be eliminated. Methods are needed to simultaneously remove or compensate impurities on the *c*-plane and nonpolar surfaces, as nonpolar planes have very different material properties from the polar *c*-planes, such as dangling bond densities, surface states, and impurities incorporation. In addition, to realize normally-OFF operation, regrowth conditions (e.g., temperature, pressure, and III/V ratio) also need to be optimized to improve acceptor concentrations at the sidewall.

IV. Conclusion

We experimentally demonstrated GaN VC-JFETs through p-GaN regrowth on the patterned fin-like channel regions by MOCVD. A subsequent photoresist self-planarization process was applied to etch away the p-GaN on top of the n-GaN fins. The regrown lateral and vertical p-n junctions were characterized to verify the effectiveness of the regrowth

process. The VC-JFETs show an ON–OFF ratio ∼100 and excellent transconductances. Devices with vertical channels aligned to ***a***-plane and ***m***-plane were also compared. The nonideal factors, such as interfacial impurities and nonuniform acceptor distribution, were also discussed. The follow-up work on minimizing leakage currents and improving BVs is underway.

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